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A Simplified Broadband Output Matching Technique for CMOS stacked Power Amplifiers

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SUMMARY   This paper describes the design method of a broadband CMOS stacked power amplifier using harmonic control over wide bandwidths in a $0.11\,\mu$m standard CMOS process. The high-efficiency can be obtained over wide bandwidths by designing a load impedance circuit as purely reactive as possible to the harmonics with broadband fundamental matching, which is based on continuous Class-F mode of operation. Furthermore, the stacked topology overcomes the low breakdown voltage limit of CMOS transistor and increases output impedance. With a 5-V supply and a fixed matching circuitry, the suggested power amplifier (PA) achieves a saturated output power of over 26.7 dBm and a drain efficiency of over 38% from 1.6 GHz to 2.2 GHz. In W-CDMA modulation signal measurements, the PA generates linear power and power added efficiency of over 23.5 dBm and 33% (@ACLR = −33 dBc).
key words: broadband, CMOS, continuous Class-F, high-efficiency, linear, power amplifier (PA), stacked transistors

1. Introduction

In today's cellular market, there is a huge demand to embed numerous wireless standards and applications into mobile communication devices. A single chip CMOS radio frequency transceiver/power amplifier (PA) with broadband characteristic is one way to reduce the cost of mass production and form factors.

Several output matching techniques for the PA, such as Class-J and continuous Class-F, have been introduced to achieve wideband operations [1], [2]. However, few studies have approached these techniques relation to the CMOS process as a result of low breakdown voltage issues. These are not well-explained in reference to the harmonic matching process.

In this work, a simplified harmonic matching technique for continuous Class-F mode of operation is presented and it is combined with a CMOS stacked topology to make an insensitive fundamental load. A description of the suggested design is given in Section 2. In Section 3, the PA was evaluated for the W-CDMA applications with continuous-wave measurement results. Section 4 summarizes the results and draws conclusions.

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2. Single-stage Continuous Class-F CMOS PA Design

An overall circuit schematic of a single-stage continuous Class-F CMOS PA is shown in Fig. 1. A quadruple-stacked FET structure is chosen to overcome low breakdown voltage problems and help ease the burden of broadband fundamental load matching [3], [4]. The gate width of each stacked transistor (TR) is 5.76 mm.

Basically, continuous Class-F PA is to control second harmonics as purely reactive as maintaining an open-circuit for third harmonic impedance. Therefore, ideal fundamental and second harmonic impedances of the continuous Class-F amplifiers are given by $Z_L = R_{opt} + j \cdot X_{opt}$, $Z_2 = -j \cdot (\pi/2) X_{opt}$ at the intrinsic drain current source [2]. In this work, a proposed output matching network is composed of a low pass filter (TL2 and C_{m5}) and a shunt resonator (TL1, C_{m3} and C_{m4}). The efficiency contours at 1.6, 1.9 and 2.2 GHz are shown at Fig. 2(a) and the low pass filter is largely helpful for synthesizing near-optimum load impedances over a wide frequency range from 1.6 to 2.2 GHz, as illustrated in Fig. 2(b). The fundamental load impedance changes smoothly from $7\,\Omega$ to $10\,\Omega$. For the practical PA design, the optimum second harmonic impedance often shifts to the
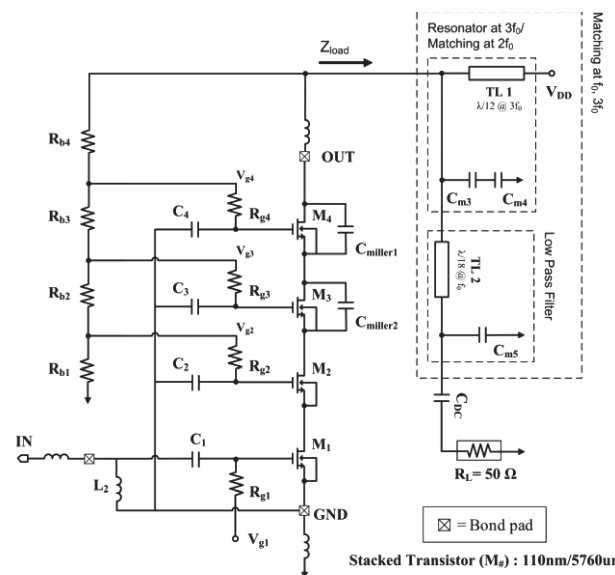

Fig. 1   Detailed Circuit Schematic of the proposed single-stage CMOS stacked PA with broadband output matching network.

inductive region due to the effect of the parasitic capacitance such as gate and drain-to-source capacitances and third harmonic impedance has to be kept purely reactive as well for continuous Class-F operation [5]. Harmonic load pull simulations were performed on this quadruple-stacked FET to confirm this and the shunt resonator with the low pass network closely moving second/third harmonic impedances to their optimum impedance points, as shown in Fig. 2(c). In addition, Miller capacitors ($C_{miller\#}$) across the drain-source

of the TRs are used to tune out the parasitic capacitance at the intermediate node of the stacked TRs to achieve high-efficiency [6], [7].

The bottom TR is in deep class-AB point with V_{GS} of 0.25 V. Three gates of stacked TRs are biased with the same gate-to-source voltage using a resistive divider with a 5-V supply. The PA is fabricated in a $0.11\,\mu m$ standard CMOS process. A chip photograph is shown in Fig. 3.

3. Measurement Results

A. Continuous Wave (CW) Measurements

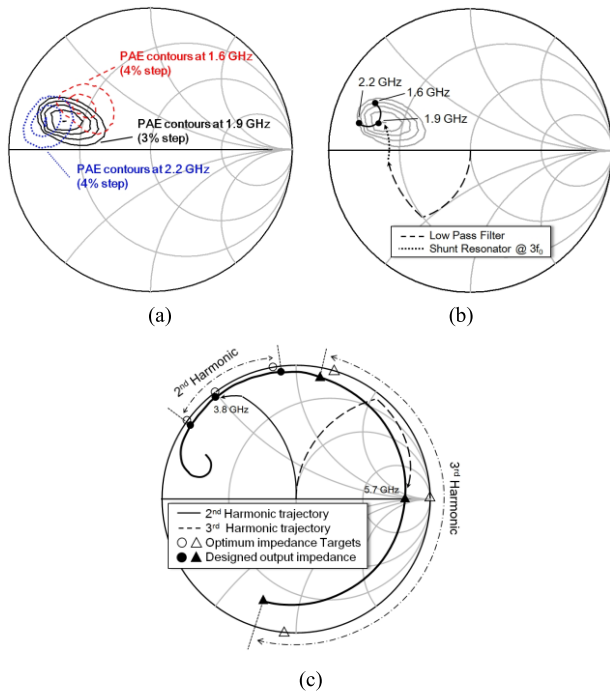In the measurement, the chip is mounted on FR-4 PCB,

Fig. 2 (a) PAE contours based on load-pull simulations at fundamental frequencies. (b) Fundamental load impedance. [1.6~2.2 GHz] (c) Simulated load impedance trajectory.
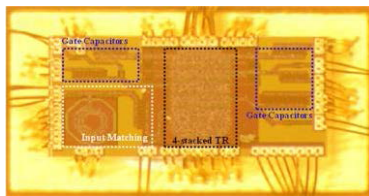

Fig. 3 Chip Microphotograph of the PA. (Die Size : $2.3 \times 1.1\,mm^2$)
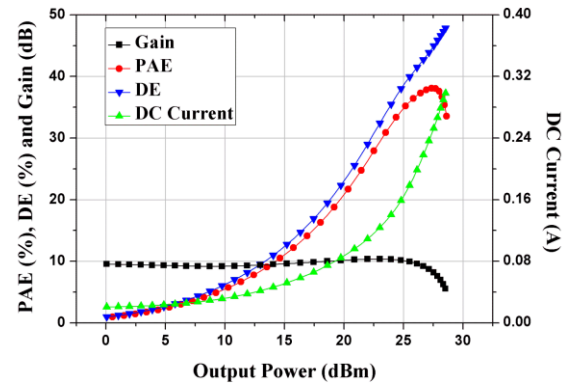

Fig. 4 Measured gain, PAE, DE and DC Current as a function of Pout with a CW input at 1.9 GHz.
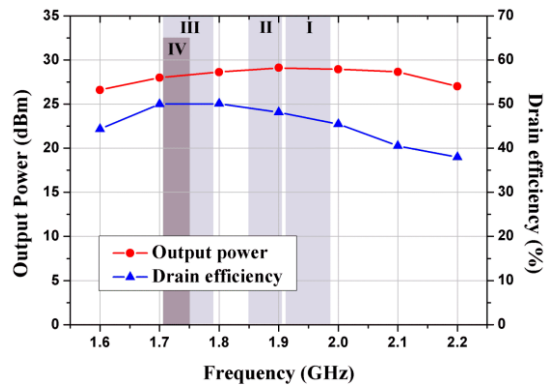

Fig. 5 Measured DE and Pout as a function of frequency; W-CDMA bands: I, II, III, and IV.

Table 1 Performance comparison of broadband linear CMOS PAs.

Ref.	Technology	Center Freq. (GHz)	P_{SAT} (dBm)	Peak PAE (%)	VDD (V)	BANDWIDTH (DE > 38%)	Linearity (P_{out}, PAE)	Modulation signal	Topology
This work	**CMOS 110 nm**	**1.9**	**29.1**	**38.2**	**5**	**600 MHz**	**24.7 dBm, 33% @ −33 dBc ACLR**	**WCDMA**	**4-stacked w/ Harmonic control**
[3]	CMOS 130 nm SOI	1.9	32.4	47	6.5	300 MHz[1]	29.4 dBm, 41.4% @ −33 dBc ACLR	WCDMA	4-stacked
[4]	CMOS 45 nm SOI	1.8	30.2	23.8	15	N/A	25.1 dBm @ −40.6 dBc ACLR	WCDMA	8-stacked cascode
[8]	CMOS 180 nm	1.8	30.8	30.6	3.3	N/A	18 dBm @ EVM = 5%	WLAN	Differential cascode w/ transformer
[9]	CMOS 65 nm	1.8	29.4	51	3.4	450 MHz[2]	25.4 dBm, 37.9% @ −33 dBc ACLR	WCDMA	stacked cascode single-differential[3]

[1]Values taken from Fig. 12 of [3], [2]Values taken from Fig. 6 (PAE > 40%) of [9], [3]External power combiner is used.

and all the losses of PCB transmission lines and bond-wires are included in the measurements. The PA was tested under a CW input at 1.9 GHz and quiescent current is 25 mA. The PA delivers 29.1 dBm output power with a power added efficiency (PAE) of 38.2% and a drain efficiency (DE) of 48.1%, as illustrated in Fig. 4.

Figure 5 demonstrates that, with a fixed matching circuitry, the output power varies less than 1 dB and the DE is above 40% from 1.7 GHz to 2.1 GHz. The PA performs 38% above a DE within the bandwidth of 600 MHz, centeredat 2 GHz.

B. W-CDMA Measurements

Figure 6 depicts the measured adjacent channel leakage ratios (ACLRs), PAE and DE performance of the PA as a function of average output power using an uplink W-CDMA signal at Band I, II and III. ACLRs were measured at 5- and 10-MHz offsets from the center frequency. ACLR were measured at 5-MHz and 10-MHz offsets from the center frequency. The average output power and PAE are larger than 23.5 dBm and 33% under the three bands, respectively when the measured ACLR at 5-MHz offset is below −33 dBc.

The PA has the best ACLR at 1.87 GHz (Band II) with an output power of 24.7 dBm. Table 1 shows the performance data of this work together with the recent broadband linear CMOS PAs for comparison.

4. Conclusion

A single-stage linear power amplifier has been proposed which has high-efficiency with broadband characteristic using the 0.11 µm standard CMOS process. The PA is based on continuous Class-F mode of operation, where output matching is realized to control the harmonic impedances to be nearly reactive using a low pass network and a shunt resonator. To avoid the problem of low breakdown voltage, stacked topology is employed, which allows the use of lower impedance transformation ratio. The presented PA achieves the output power of 29.1 dBm at 1.9 Hz and DE over 38% for the operating frequency band. For a W-CDMA modulated signal, the maximum linear output power is 24.7 dBm and the PAE is 33% at 1.87 GHz. These results show the proposed linear CMOS PA is useful for broadband and high-efficiency applications.
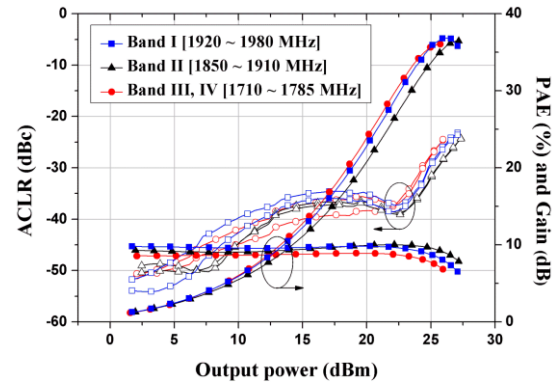
Acknowledgments

Fig. 6 Measured performance of proposed PA for broadband operation with W-CDMA signal.

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