A Reconfigurable Dual-Band CMOS Power Amplifier With an Integrated Switchable Transformer

[1]Jaeyong Ko, [2]Sangwook Nam
INMC & Department of Electrical and Computer Engineering
Seoul National University
Seoul, Korea
[1]sciencedo@ael.snu.ac.kr, [2]snam@snu.ac.kr

***Abstract*—An integrated switchable transformer for a reconfigurable dual-band power amplifier (PA) is presented. The single dual-band PA is fully integrated using a 0.18-µm RF CMOS process. The reconfigurable transformer is designed by tuning its primary winding and a shunt capacitor at 50 ohm load. This single PA operates in the S/X-bands and simulated results show a 1-dB compression output power (P1dB) of 20.5 dBm and 20.63 dBm with a power-added-efficiencies (PAE) of 17.4% and 12.72% at 3.5 GHz and 9.0 GHz, respectively. The 1-dB bandwidth is 2.4 GHz (7.0-9.4 GHz) for the X-band and 0.2 GHz (3.45-3.65 GHz) for the S-band. This amplifier with the switchable transformer can be used for integration in a dual-band high-resolution radar transceiver.**

Keywords—CMOS, dual-band, power amplifier (PA), radar transceiver, reconfigurable, switchable transformer.

I. INTRODUCTION

To allow the interpretation of complex scenes, multi-band radars take advantage of the differing characteristics of environment and targets according to exploited carrier frequencies. For example, signals in the S-band have strong immunity against severe weather and atmospheric attenuation. On the other hand, frequencies in the X-band are often used for highly resolved target imaging [1], [2]. Achieving dual-band functionality has been challenging, especially for fully integrated CMOS power amplifiers (PAs), due to low breakdown voltage and a low quality-factor. Most updated multi-band PAs are not appropriate for radar systems because the aforementioned frequency bands are far apart and multiple PAs are optimized at each target frequency [3].

There have been several approaches to implement multi-band and broadband characteristics in a single PA. One approach is to employ a transformer-based high-order output matching network or a stacked stepped-impedance (SSI) transformer to accomplish the wideband operation [4], [5]. However, using this approach, it was found that passive efficiency rapidly decreases and load matching cannot be maintained at lower bands. Some studies have used parallel/series resonant LC structures or an off-chip combiner [6], but these approaches are not suitable for single-chip integration and low-cost implementation.

In this paper, we propose a single dual-band PA with a reconfigurable output matching network. The dual-band matching network is realized by introducing a switchable transformer that can tune the primary inductance of the transformer, and a shunt capacitance at 50 ohm load. Since the highest peak efficiencies of the designed transformer are 57% and 71% for S/X-band operation, the dual-band PA delivers a 1-dB compression output power (P1dB) of over 20 dBm and a maximum power-added-efficiency (PAE) of over 20% with 1.8V/3.6V supply for driver/main amplifier.

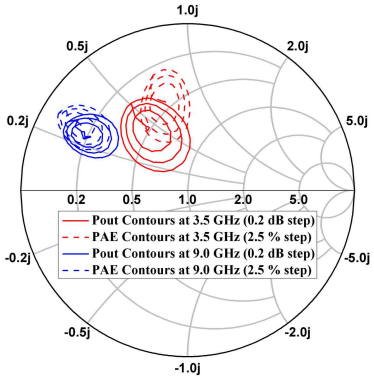


Fig. 1. Simulated load-pull contours at 3.5 GHz and 9.0 GHz.

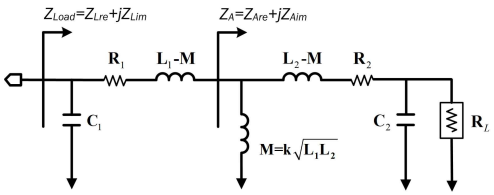


Fig. 2. Equivalent circuit for the on-chip transformer.

II. DESIGN OF DUAL-BAND CMOS PA

A. Impedance Transformation

For a given power device and technology, the maximum output voltage is constrained by the device's breakdown and the maximum output current is limited by the device size and input voltage drive. Assuming class-A operation, for maximum output power from a given device, the optimum load presents an equivalent inductance L_p to resonate with the

device nonlinear output capacitance C_{device} at the operating frequency w and a parallel resistive part R_{opt}, determined by the following two equations:

$$jwL_P = \frac{-1}{jwC_{device}} \quad (1)$$

$$R_L = R_{opt} \approx \frac{V_{\max} - V_{knee}}{I_{\max}} \quad (2)$$

where V_{knee} represents the finite knee voltage of the power device. Given that R_{opt} and C_{device} are independent of the operating frequency as in [7], the optimum load impedance moves on a conductance circle with $1/R_{opt}$ (Fig. 1) and a smaller L_p is required as the frequency increases. This scenario is quite different from a situation with multi-mode operation for back-off efficiency [8].

In this paper, a high-Q transformer and additional capacitors (C_1 and C_2) are used for an output matching network, its equivalent circuit is shown in Fig. 2. L_1 and L_2 are the primary and secondary winding inductances of the transformer, respectively. R_1 and R_2 represent the parasitic resistances of the primary and secondary windings, respectively. M represents the mutual inductance of L_1 and L_2. Z_{Load} of Fig. 2 can be calculated as follows:

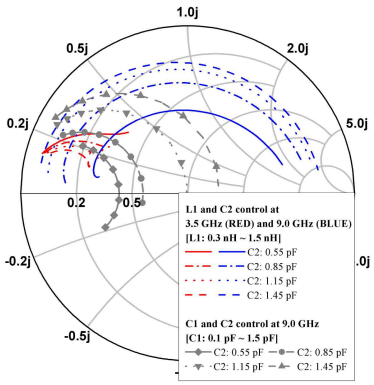


Fig. 3. Normalized Z_{Load} with the variations of L_1, L_2, C_1 and C_2 at 3.5 GHz and 9.0 GHz.

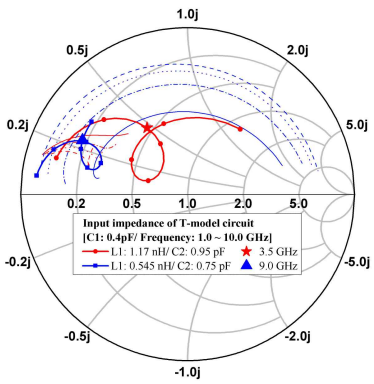


Fig. 4. Normalized Z_{Load} with the optimized L_1, L_2, C_1 and C_2 according to frequency (1.0-11.0 GHz).

$$Z_{Load} = [Z_A + jw(L_1 - M) + R_1] \| \frac{1}{jwC_1}. \quad (3)$$

Assuming the coupling factor k is 0.7 and the parasitic resistances of the windings are expressed as $R_1=wL_1/Q$ and $R_2=wL_2/Q$ while the quality factor (Q) is 10, the transformed impedance Z_{Load} was simulated for the two cases and illustrated in Fig. 3. First, Z_{Load} is calculated with varying C_1 and C_2 at 9.0 GHz when C_1 and C_2 vary from 0.1 to 1.5 pF and from 0.55 to 1.45 pF, respectively. With the selection of L_1 (0.545 nH) and L_2 (1.11 nH), the matching network cannot provide optimum load impedance for the S-band. Second, Z_{Load} is calculated with varying L_1, C_2 and fixed C_1 (0.4 pF) for each band when L_1 and C_2 range from 0.3 to 1.5 nH and from 0.55 to 1.45 pF, correspondingly. If L_1 is increased for the lower-band, the real and imaginary part of Z_{Load} is increased while C_2 provides precise control of Z_{Load} at optimum load impedance. Therefore, L_1 and C_2 are designed to be switchable to yield optimum Z_{Load} at the S- and X-bands, as shown in Fig. 4.

B. Reconfigurable Dual-Band Transformer

In this section, we suggest a switchable transformer for a dual-band matching network. The proposed reconfigurable matching network (illustrate in Fig. 5) employs two switches, S1 and S2, to realize optimum impedances of the S/X-bands. S1 is located on the primary winding of the transformer, and is connected in parallel to an additional inner winding. S2 is applied to a shunt capacitor in series, which is connected to the secondary winding of the transformer. The switchable transformer is embodied as shown in Fig. 6(a). The primary part is split into two lines and intertwined around the two parallel-connected secondary parts to improve the coupling factor. With the inner turn inductor, the primary inductance increases for the lower-band. In order to avoid the generation of parasitic capacitance, there exists a gap of 29 um between the secondary winding and the inner turn inductor, which keeps the high efficiency at the higher band. Details for the designed transformer are presented in Table. I.

For the X-band, S1 is turned on and S2 is turned off to achieve low load impedance. On the other hand, S1 is turned off and S2 is turned on for the S-band. When designing the switchable matching network, two main issues related to handling with high-power should be considered. One is the capability of power-handling for the OFF-state and the other is the power loss from parasitic resistances of the switches in the

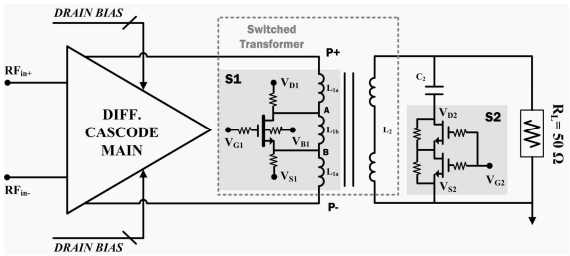
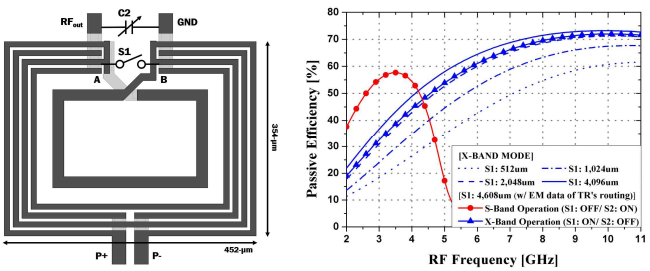


Fig. 5. Schematic of the reconfigurable dual-band output matching network with one single PA.



(a) (b)

Fig. 6. (a) Physical layout of the output matching network. (b) Passive efficiency for each band operation.

TABLE I. DETAILS FOR THE DESIGNED TRANSFORMER

Primary width (M6)	*Secondary width (M6)*	*Inner primary width (M5&M6)*	*Spacing*	*Top metal thickness*
10 um	10 um	20 um	6 um	Al-4.6 um

TABLE II. BIAS CONDITIONS ACCORDING TO THE BANDS

Band	V_{D1}, V_{S1}	V_{B1}	V_{G1}	V_{S2}, V_{B2}	V_{G2}
S-band	VDD	1.0 V	1.0 V	GND	3.0 V
X-band	VDD	1.0 V	6.0 V	GND	-2.0 V

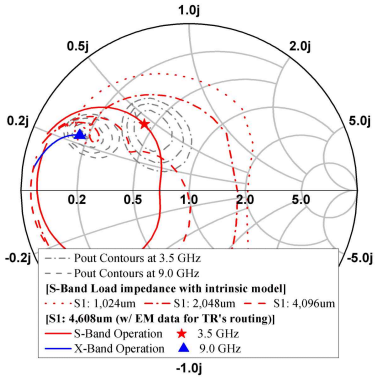


Fig. 7. Normalized Z_{Load} of the designed transformer in compliance with frequency (2.0-11.0 GHz).

ON-state. For the OFF-state of S1 and S2, V_{A-B} and V_{D2} are nearly 4V, so the switches can be implemented as a single thick gate-oxide transistor. However, S2 was implemented by two stacked thin-gate transistors to reduce the parasitic capacitance. When considering the gate width of transistors due to on-resistance (R_{on}), the parasitic capacitance (C_{ds}) cannot be ignored for the OFF-state. The trade-off of R_{on} and C_{ds} results in an optimum device width and balances the effects, as shown in Fig. 6(b) and Fig. 7. The gate width of transistor S1 is 4.608 mm with a length of 0.35-μm, which has C_{ds} of 1.8 pF and R_{on} of 0.6 Ω. The passive power efficiencies of the transformer with S1 are 57% and 71% at 3.5 GHz and 9.0 GHz, respectively, which are competitive with other results [9]. For the two series-connected transistors of S2, the gate width of each transistor is 1.12 mm with length of 0.18-μm. The OFF-state capacitance of the two-stacked transistors is 0.35 pF. The bias conditions according to each band are described in Table. II.

C. Circuit Schematic of the Two-Stage Dual-Band PA

The circuit schematic of the two-stage reconfigurable dual-band CMOS PA with the proposed output matching network is presented in Fig. 8. A differential cascode structure is applied to the driver and main stage to moderate the voltage stress in each transistor, which has a low breakdown voltage, and to achieve a larger gain. Although the differential cascode topology can reduce the effects of the bonding wires at the source of the common source, the dual-band PA presented here employs series-resonance circuits for the higher band in order to alleviate the asymmetric effects of the output matching network. For the driver stage, the gate length of transistors is 0.18-μm, and each total gate widths of the common source/gate are 648 um with a supply of 1.8V. For the main stage, the total gate widths of the common source/gate are 1024/1152 um with gate length of 0.18/0.35-μm with a supply of 3.6V.

A common source switch with a series capacitor is designed for the reconfigurable dual-band operation and this combination is applied to input and inter-stage matching. For the S-band, SW1 and SW2 are turned on and the inter-stage matching network is composed of a shunt inductor, a series capacitor and a parallel resonance. In the OFF-state for SW1 and SW2, a series capacitor among two parallel shunt inductors is shown at the inter-stage matching network for the X-band. Each gate width of SW1 and SW2 with the thin oxide is optimized as 256 um and 1152 um, respectively. The SW2 has C_{ds} of 0.53 pF and R_{on} of 0.6 Ω. Additionally, a deep N-well is employed in all transistors of the PA to reduce the noise and signal coupling with other components on the

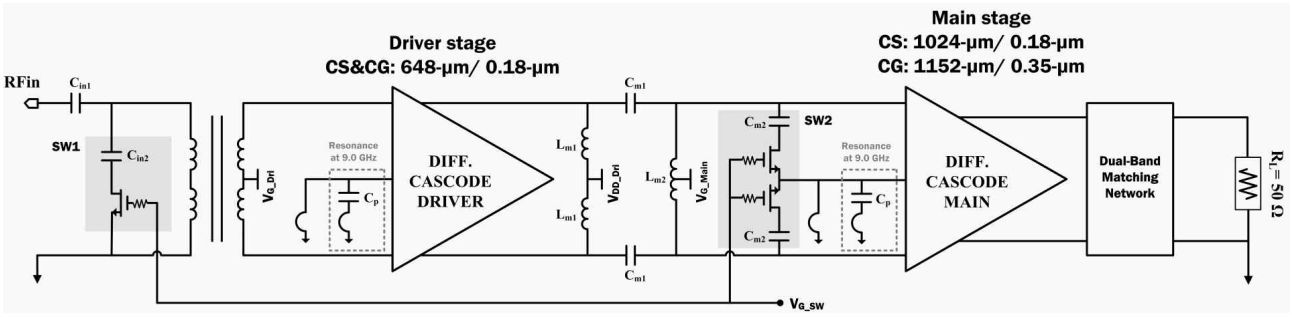


Fig. 8. Schematic of the two-stage reconfigurable dual-band CMOS PA.

silicon substrate.

III. Simulation Results

The proposed S/X dual-band PA is fully implemented in 0.18-µm 1P6M RF CMOS process which provides 4.6 um-thick aluminum as a top metal and MIM capacitors with 2.0 fF/mm^2. For the S-band, the amplifier consumes 99 mA of DC current: that is, 78 mA for the power stage, and 21 mA for driver stage are drawn. For the X-band, the total DC current is 148 mA: 109 mA for the power stage and 39 mA for the driver stage. The load impedances of the proposed output matching network applied to the dual-band PA are presented in Fig. 9 for switches' operation and located well at targeted load impedances.

Fig. 10 shows that 1-dB compression output power is 20.5 dBm and 20.63 dBm, with PAE of 17.4% and 12.72% at 3.5 GHz and 9.0 GHz, respectively. For both two frequencies, a saturated output power (P_{sat}) is more than 21 dBm and a max PAE is more than 20%. As illustrated in Fig. 11, the 1-dB bandwidth is 0.2 GHz (3.45–3.65 GHz) for the S-band and 2.4 GHz (7.0–9.4 GHz) for the X-band. In comparison with the other fully integrated CMOS PAs operating in the X-band, this amplifier shows competitive simulation results even though it achieves dual-band function.

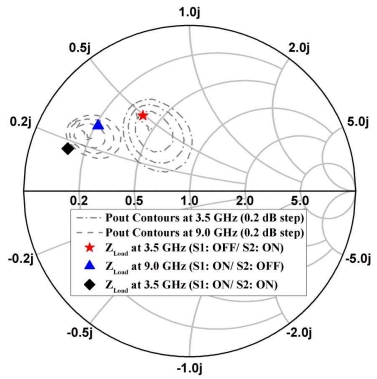


Fig. 9. Normalized Z_{Load} with respect to the switches' operation.

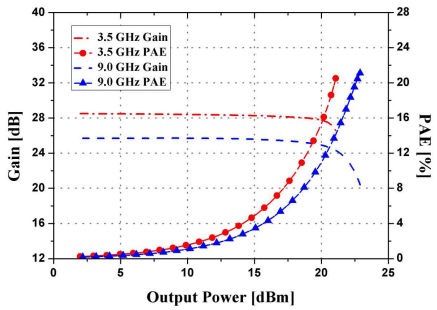


Fig. 10. Simulated gain, PAE as a function of Pout with a CW input at 3.5 GHz and 9.0 GHz.

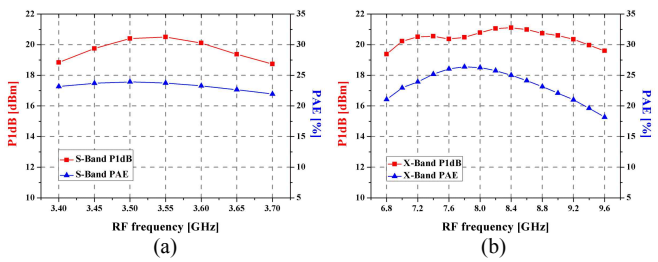


Fig. 11. Simulated P1dB and PAE versus frequency. (a) S-Band (b) X-Band.

IV. Conclusion

In this paper, a single reconfigurable dual-band PA is fully integrated in 0.18-µm 1P6M RF CMOS technology. An integrated switchable transformer, which is a key element of the PA, was studied in terms of an equivalent circuit, optimum load matching, efficiency, transistors for high-power switches and so on. The suggested PA, which consists of two differential stages with input, inter-stage, and output matching network, operates at S/X-bands. Simulation results show that a P1dB of 20.5 dBm and 20.63 dBm with PAE of 17.4% and 12.72% at 3.5 GHz and 9.0 GHz, respectively. Additionally, the PA provides a P_{sat} of over 21 dBm and a max PAE of 20% for the S/X-band. The simulated 1-dB bandwidth is 0.2 GHz (3.45-3.65 GHz) and 2.4 GHz (7.0-9.4 GHz) for the S- and X-band, respectively. Considering the specifications, this amplifier is possibly suitable for use in a dual-band high-resolution radar system.

Acknowledgment

This work was supported by the Brain Korea 21 Plus Project in 2016.

References

[1] Y.-K. Kwag, J.-S. Jung, I.-S. Woo and M.-S Park, "Modern software defined radar (SDR) technology and its trends," *Journal of Electromagnetic Engineering and Science*, vol. 14, no. 4, pp. 321–328, Dec. 2014.

[2] J F. Scotti, F. Laghezza, P. Ghelfi, and A. Bogoni, "Multi-band softwaredefined coherent radar based on a single photonic transceiver," IEEE Trans. Microw. Theory Tech., vol. 63, no. 2, pp. 546–552, Feb. 2015.

[3] W.-Y. Kim, H. S. Son, J. H. Kim, J. Y. Jang, I. Y. Oh, and C. S. Park, "A fully integrated triple-band CMOS class-E power amplifier with a power cell resizing technique and a multi-tap transformer," IEEE Microw. Wireless Compon. Lett., vol. 23, no. 12, pp. 659–661, Dec. 2013.

[4] H. Wang et al., "A CMOS broadband power amplifier with a transformer-based high-order output matching network," IEEE J. Solid-State Circuits, vol. 45, no. 12, pp. 2709–2722, Dec. 2010.

[5] H J. Qian, J O. Liang, and X. Luo, "Wideband digital power amplifiers with efficiency improvement using 40-nm LP CMOS technology," IEEE Trans. Microw. Theory Tech., vol. 64, no. 3, pp. 675–687, Dec. 2015.

[6] J. Choi, B. Kim, D. Kim, J. Ko and S. Nam, "A dual band CMOS power amplifier for an S/X band high resolution radar system," in Proc. IEEE Radio Frequency Integrated Circuits Conf., pp. 335–338, June 2014.

[7] S. Cripps, Advanced Techniques in RF Power Amplifier Design. Norwood, MA: Artech House, 2002.

[8] Y. Cho, B. Park, S. Jin, J. Kim, K. Moon, D. Kang, H. Jin, S. Koo, and B. Kim, "Transformer based dual-power-mode CMOS power amplifier for handset applications," in. 44th Eur. Microw. Conf., pp. 436–439, Oct. 2014.

[9] J.P. Comeau, E.W. Thoenes, A. Imhoff, and M.A. Morton, "X-band +24 dBm CMOS power amplifier with transformer power combining," in Proc. Silicon RF Symp., pp.49–52, Jan. 2011.