# Low-Spurious Wideband DDS-Based Ku-Band Chirp Generator for Short-Range Radar Application

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***Abstract*—Direct digital synthesizer (DDS)-based chirp generator is a popular component in high-performance radar systems owing to its high speed and excellent chirp-linearity properties. This letter presents a 12–18 GHz DDS-based chirp generator with high spectral purity by proposing a method for planning the optimal frequencies. To verify the performance, the RF characteristics of the fabricated chirp generator were measured, and range profile measurements were performed to test the fabricated chirp generator.**

***Index Terms*—Direct digital synthesizer (DDS), frequency-modulated continuous wave (FMCW) waveform generation, frequency planning, short-range radar.**

## I. Introduction

NOWADAYS, direct digital synthesizer (DDS)-based chirp generator is widely used to achieve flexibility, high-frequency resolution, linearity, and speed [1]. Although commercial DDSs are available, designing a DDS using field-programmable gate array (FPGA) and high-speed digital-to-analog converter (DAC) is preferred for its advantages—it is easier to synchronize and reconfigure waveform. There are some disadvantages as well, such as a relatively narrow bandwidth and low spectral purity. To overcome these shortcomings, co-design of digital multiple DDS architecture (multi-DDS) and RF frequency conversion module has been proposed [2]–[4]. The multi-DDS functions to generate a baseband chirp signal with a bandwidth above the Nyquist limit for the FPGA clock frequency. It generates the chirp signal in parallel, serializes it, and feeds it to the high-speed DAC. Then, the RF frequency conversion module converts the baseband chirp signal to a higher and broader chirp signal. It usually comprises multiple frequency multipliers and RF filters [4]–[7], occasionally using an extra mixer to shift the frequency band [2], [3], [8]. However, going through these multiple RF components can create additional spurious signals; therefore, optimized frequency planning is required to minimize them.

Manuscript received January 15, 2022; accepted February 1, 2022. Date of publication February 9, 2022; date of current version March 11, 2022. This work was supported in part by the North Atlantic Treaty Organization (NATO) Science for Peace and Security Program under Grant G5395 (http://www.nato.int/science). *(Corresponding author: Sangwook Nam.)*

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Color versions of one or more figures in this letter are available at https://doi.org/10.1109/LMWC.2022.3149244.
Digital Object Identifier 10.1109/LMWC.2022.3149244

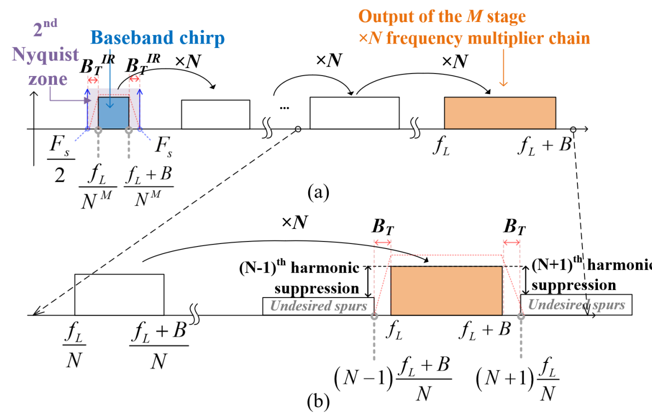


Fig. 1. Spectrum of a super-Nyquist architecture with an $M$ stage $\times$ $N$ frequency multiplier chain. (a) Simplified spectrum at all frequencies. (b) Spectrum of a single stage of the frequency multiplier chain.

This letter presents a low-spurious wideband DDS-based chirp generator design method based on frequency planning. Then, the fabricated Ku-band chirp generator and its performance are introduced. Finally, the functionality of the proposed chirp generator is verified through range-profile measurements using the in-house Ku-band FMCW radar prototype.

## II. Optimal Frequency Planning

In the design proposed in this letter, the super-Nyquist architecture [9] with mix-mode DAC, where the multi-DDS generates a signal in the second Nyquist zone, is used to simplify the RF stages. As shown in Fig. 1(a), a baseband chirp generated in the second Nyquist zone of the DAC is converted to an RF chirp with the lowest frequency $f_L$ and bandwidth $B$ at the output of the $M$ stage $\times$ $N$ frequency multiplier chain. Each frequency multiplier generates undesired harmonic leakages. To filter out these leakages, the desired harmonic band should not overlap with the undesired harmonic bands as depicted in Fig. 1(b), which yields

$$f_L - (N-1)\frac{f_L + B}{N} > B_T \quad (1)$$

$$(N+1)\frac{f_L}{N} - (f_L + B) > B_T \quad (2)$$

where the transition band of the RF bandpass filter $B_T$ can be expressed as a fraction of signal bandwidth $B$ as $B_T = p_1 B$. From (1) and (2), the necessary condition to filter out all the undesired harmonics can be derived as

$$f_L \geq N(1 + p_1)B > 2B \quad (3)$$

where $N$ is an integer not less than 2. As shown in Fig. 1(a), through the condition which filters out the DAC clock leakage signals and out-of-band signals, the additional relations are obtained as

$$\frac{f_L}{N^M} - \frac{F_s}{2} > B_T^{IR} \tag{4}$$

$$F_s - \frac{f_L + B}{N^M} > B_T^{IR} \tag{5}$$

where the transition band for image-rejection filter $B_T^{IR}$ can be expressed as a fraction of the DAC sampling rate $F_s$ as $B_T^{IR} = p_2 F_s$. From (4) and (5), the upper bound for the DAC sampling rate can be obtained with the condition of existence of the cascaded multiplier factor $N^M$, which yields

$$F_s < \frac{(1 - 4p_2) f_L - (1 + 2p_2) B}{(1 + 2p_2)(1 - p_2)}. \tag{6}$$

Furthermore, to effectively eliminate the images and DAC sampling clock leakages with a bandpass filter, the center frequency of the baseband chirp is chosen as the center of the second Nyquist zone, which yields

$$F_s = \frac{4(f_L + 0.5B)}{3N^M}. \tag{7}$$

From (6) and (7), we can determine the multiplication factor $N$, the number of frequency multipliers $M$, and DAC sampling rate $F_s$. Note that the parameters $M$ and $F_s$ should be chosen with careful consideration of the trade-offs between digital and RF design complexity. When the selected DAC sampling rate $F_s$ is close to the upper bound, both the complexity of the DAC and the number of DDS blocks in the multi-DDS increase, which can be a burden on the FPGA. In contrast, the required frequency multipliers increase when the value of the selected DAC sampling rate $F_s$ is too low.

Given the required chirp specifications $f_L$ and $B$, all design parameters ($F_s$, $M$, $N$, $p_1$, and $p_2$) can be obtained by pre-determining two of these parameters and using (3), (6), and (7). The pre-determined parameters and their values should be selected by considering the actual implementation. If the system requires a fractional bandwidth (FBW) of more than $[200/(2N + 1)]$ %, the chirp specifications $B$ and $f_L$ violate (3). Especially if the system requires FBW of more than 40%, (3) cannot be met regardless of the multiplication factor $N$. Thus, the output frequency of the $M$ stage frequency multiplier chain should be adjusted as

$$f_L^{\mathrm{NEW}} = f_L + f_{\mathrm{shift}} \tag{8}$$

where $f_L^{\mathrm{NEW}}$ is the new output frequency of the frequency multiplier chain, $f_L$ is the required lowest frequency of the chirp signal, and $f_{\mathrm{shift}}$ is the frequency of the single-tone signal for the frequency shifting. Thus, a wideband down-conversion mixer is needed after the $M$ stage frequency multiplier chain in order to implement the frequency shifting operation of (8). Then, given the chirp specifications $f_L$, and $B$, the other design parameters ($f_{\mathrm{shift}}$, $F_s$, $M$, $N$, $p_1$, and $p_2$) can be obtained by pre-determining three of them and replacing $f_L$ in (3), (6), and (7) with $f_L^{\mathrm{NEW}}$ in (8). Note that the down-conversion mixer can cause other spurious signals. They can be suppressed by reducing the input power to the mixer, but this strategy may require an additional gain block at the output RF path to meet the output power requirement.

TABLE I
DESIGN PARAMETERS OF THE KU-BAND CHIRP GENERATOR

| Parameter | Value | Grounds |
|---|---|---|
| $F_s$ | *3.93216 GHz | According to (6), (7), and (8) |
| $f_{shift}$ | 8.38 GHz | According to (3), (6), and (8) |
| $M$ | 3 | According to (7) and (8) |
| $N$ | 2 | Pre-determined in consideration of COTS |
| $p_1$ | 0.667 | Pre-determined in consideration of COTS |
| $p_2$ | 0.1 | Pre-determined in consideration of COTS |

* $F_s$ was slightly adjusted to be a multiple of the external PLL output frequency.

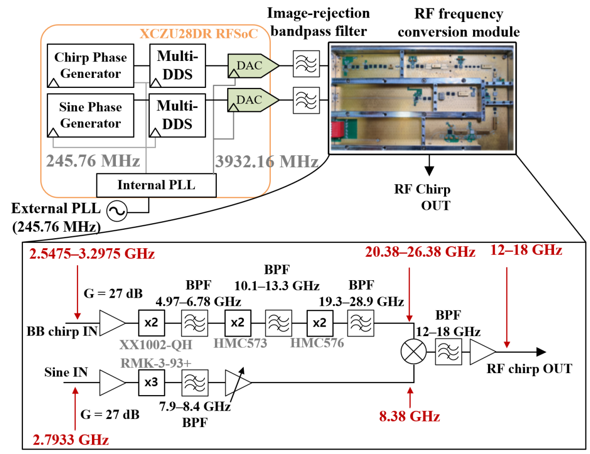


Fig. 2. Block diagram of the implemented Ku-band chirp generator.

## III. IMPLEMENTATION OF THE KU-BAND CHIRP GENERATOR

As shown in Fig. 2, the Ku-band chirp generator ($f_L = 12$ GHz, $B = 6$ GHz) was realized using the design parameters (see Table I) obtained by the proposed frequency planning method. For the digital part, the XCZU28DR RFSoC platform HTG-ZRF8 [10] was used to implement the multi-DDS and mix-mode DAC. The multi-DDS was implemented using the Xilinx logiCORE IP DDS compiler. For the RF part, the frequency conversion module was manufactured using commercial off-the-shelf (COTS) chips and a four-layer PCB with Rogers RO4003 and FR-4. Active frequency multipliers were used in the frequency multiplier chain to minimize the gain block, reducing hardware complexity and cost. Moreover, the appropriate insertion losses in the filter blocks were intended to satisfy the input power requirement of each frequency multiplier and reduce the multiple reflections caused by the impedance mismatches.

The output specifications of the implemented chirp generator are characterized as the spurious-free dynamic range (SFDR), output power spectrum, phase noise, and spectrogram. The measurements were performed using the spectrum analyzer (E4440A) and digital oscilloscope (MSO73304DX). The measurement results in Fig. 3 indicate the performance with 11 dBm output power, averaged SFDR level of 45.5 dBc, and phase noise of −105 dBc/Hz at an offset of 1 MHz from the 15 GHz carrier. As mentioned in Section II, the SFDR was

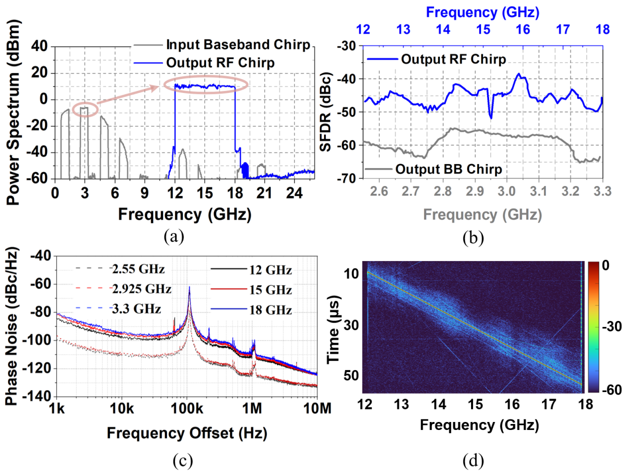


Fig. 3. Measured performance of the implemented Ku-band chirp generator. (a) Power spectrum, (b) SFDR, (c) phase noise of the baseband and RF chirp at 12/15/18 GHz, and (d) normalized spectrogram of the 6-GHz/50-$\mu$s chirp.

TABLE II

COMPARISON OF DDS-BASED CHIRP GENERATOR SPECIFICATIONS

| Ref. | $f_L$ (GHz) | $B$ (GHz) | FBW (%) | RF architecture | $f_L^{NEW}$ (GHz) | SFDR (dBc) |
|---|---|---|---|---|---|---|
| [2] | 2 | 16 | 160 | ×16 *FMC + 20G *DCM | 22 | −15 (Worst) |
| [3] | 2 | 6 | 120 | ×8 FMC + 10G DCM | 12 | Not provided |
| [4] | 12 | 6 | 40 | ×8 FMC | - | Not provided |
| [5] | 90 | 10 | 10 | ×12 FMC | - | Not provided |
| [6] | 1.42 | 5.3 | 31 | ×8 (N=2, M=3) FMC | - | −53 |
| [7] | 15.9 | 1.5 | 9 | 4.8 G *UCM + ×3 ($N$=3, $M$=1) FMC | - | −41 |
| [8] | 0.8 | 5.2 | 153 | 7.9G UCM + ×4 ($N$=4, $M$=1) FMC + 31.4G DCM | 32.2 | −48 (Avg.) |
| **This work** | **12** | **6** | **40** | **×8 ($N$=2, $M$=3) FMC+8.38G DCM** | **20.38** | **−38 (Worst) −45.5 (Avg.)** |

*FMC: Frequency multiplier chain
*DCM: Down-conversion mixer
*UCM: Up-conversion mixer

slightly degraded at around 16 GHz by the down-conversion mixer. Other than that, the SFDR and the phase noise at Ku-band are originated from the baseband signal. When going through three frequency doublers, the SFDR is degraded by 18.06 dB since the spurious level increases by 6.02 dB through each frequency doubler [11]. According to the phase noise propagation model going through the frequency multipliers and the mixer [12], the phase noise is also degraded by the following relation:

$$S_{\varphi_{\text{out}}}(f) = \left(N^M\right)^2 S_{\varphi_{\text{BB}}}(f) + S_{\varphi_{\text{shift}}}(f) \tag{9}$$

where $S_\varphi(f)$ is the power spectral density of the phase noise $\varphi(t)$. Considering the assumption that the phase noises of the chirp and single-tone sources are perfectly correlated, it can be deduced that the phase noise of the RF output increases by at least 13.98 dB.

To further investigate the validation of the proposed frequency planning, the DDS-based chirp generators are compared in Table II. In [7] and [8], a commercial DDS and an up-conversion mixer were used instead of the super-Nyquist architecture. It is confirmed that a down-conversion mixer was mostly used when the FBW of 40% and more is required [2], [3], [8]. Furthermore, the chirp generators which satisfy the proposed conditions, especially (3) and (8), provide excellent SFDR characteristics [6]–[8].

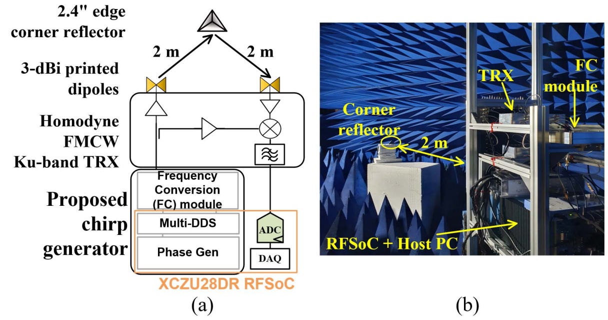


Fig. 4. Range profile measurement setup in an anechoic chamber. (a) Block diagram and (b) photograph of the measurement environment.

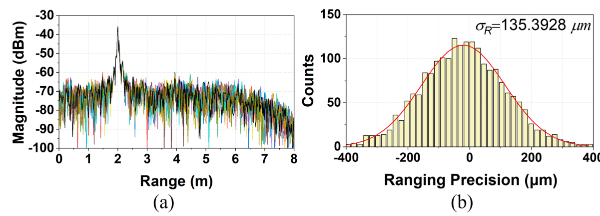


Fig. 5. Results of the range profile measurement. (a) Range profile for the ten measurements and (b) ranging precision from the 2048 measurements.

Using 6-GHz/50-$\mu$s chirp as shown in Fig. 3(d), the range profile measurements were performed to test the functionality of the fabricated chirp signal. As shown in Fig. 4, a 2.4″ edge trihedral corner reflector was placed 2 m apart from the radar platform. The in-house homodyne FMCW Ku-band TRX, 3-dBi printed dipoles were used to transmit and receive the RF signal. Furthermore, the data acquisition system was implemented with the multi-DDS in the RFSoC to synchronize the system. Regarding the post-processing, the TX-to-RX coupling signal and clutter signals were removed by subtracting with the signal obtained in the absence of the target. The range profiles for the multiple measurements are plotted in Fig. 5(a). The results indicate that the target is placed at 2 m apart from the radar. After applying the Hamming window, the measured SNR is 14 dB, and the measured range resolution is 3.66 cm. In addition, the ranging precision was obtained with the 2048 measurements to investigate the various noise source effects on the measurement [13], [14]. As shown in Fig. 5(b), the system ensures the ranging precision of 135.39 $\mu$m which is close to the Cramer-Rao lower bound of the ranging precision (48) in [13] of 109 $\mu$m.

## IV. CONCLUSION

This letter has proposed a design method for a low-spurious and wideband chirp generator using a super-Nyquist architecture and a multistage frequency multiplier chain. The distinctive contribution of this study is that it has presented the derivation of the optimal design parameters that provide low-spurious characteristics based on frequency planning. This method was validated by fabricating the Ku-band chirp generator with a spurious level with the averaging level of −45.5 dBc.

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