제37권 제1호 Volume 37. Number 1

2014년도

마이크로파 및 전파전파 합동학술대회

논문집

일 시_ 2014년 5월 24일

장 소_ 한발대학교

주 최_ 한국통신학회 마이크로파 및 전파 연구회
전파 엔지니어링랩

후 원_ (주) 창성, 애드모텍, 에이스테크놀로지,
담스테크, HCT, 맨앤텔

협 찬_ 알트소프트, 이너트론, 에이스웨이브텍

Session B

Linearity improvement for Broadband CMOS stacked Power Amplifiers With integrated Adaptive bias Circuit

Jaeyong Ko°, Dooheon Yang and Sangwook Nam

School of Electrical Engineering, and INMC, Seoul National University

sciencedo@ael.snu.ac.kr

I. INTRODUCTION

In modern smart handheld devices, there is an explosive demand to handle an increased amount of information and content using the limited available frequency spectrum, such as LTE and worldwide inter-operability for microwave access (WIMAX). Since the modulated signals have high peak-to-average-power ratios (PAPR) with wide bandwidths, PAs should be operated at a back-off power from the peak to satisfy the linearity. Due to the serious level of efficiency degradation from the back-off operation, the linearization technique is crucial at a high power region.

II. DESIGN AND RESULTS

This paper applies an adaptive bias circuit to the bottom-TR of a stacked PA to improve linearity, using the 0.11-μm RF CMOS process. By using the bias circuit, as illustrated in Fig. 1, a sweet spot and peak average output power can be located as a deeper class-AB bias without any linearity distortion at the low-to-mid power region [1]. Considering bandwidth and output power, a stacked topology is employed in this paper and it is composed of four connected transistors in a series, as shown in Fig. 2 [2]. In Fig. 3, the PA with the integrated bias circuit improves 5 dB at the sweet spot of $ACLR_{E\text{-}UTRA}$, compared to the constant Class-AB bias PA and shows an average output power of 25.3 dBm, a PAE and DE of 21/29 %, with an $ACLR_{E\text{-}UTRA}$ of -30 dBc at 1.88 GHz for a LTE 10 MHz 16 QAM 7.5dB PAPR signal. Also, The PA delivers an average output power and

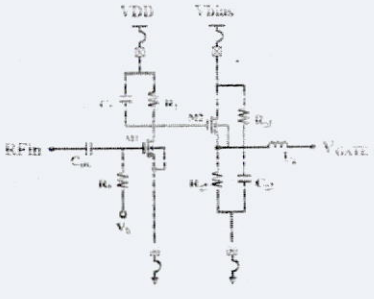

Fig. 1. Schematics of the adaptive bias circuit for the gate of the Bottom-TR.

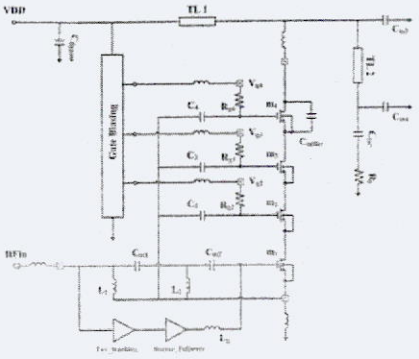

Fig. 2. Overall schematic of broadband 4-stacked PA with the adaptive bias circuit.

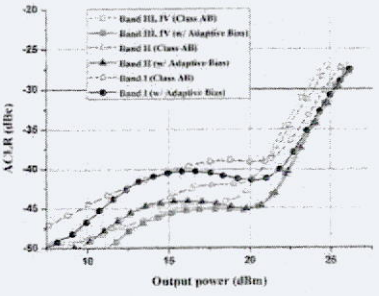

Fig. 3. Measured ACLRs of the designed PA using LTE signal at band I, II, III, and IV.

DE more than 24.5 dBm/25.6 % from 1.55 GHz to 2.05 GHz with the same bias condition. This adaptive bias circuit applied to a stacked PA is useful for broadband linear applications.

ACKNOWLEDGEMENT

This research is supported by Dongbu HiTek, Seoul, Korea.

REFERENCES

[1] S. Jin, B. Park, K. Moon, Y. Cho, D. Kim, H. Jin, J. Park, and B. Kim,"Enhanced linearity of CMOS power amplifier using adaptive common gate bias control," in Proc. IEEE MTT-S Int. Microw. Symp. Dig., Jun. 2013, pp. 1–4.

[2] S. Pornpromlikit, J. Jeong, C. D. Presti, A. Scuderi, and P. M. Asbeck, "A watt-level stacked-FET linear power amplifier in silicon-on-insulator CMOS," IEEE Trans. Microw. Theory Tech., vol. 58, no. 1, pp. 57–64, Jan. 2010.