2014년도

# 마이크로파 및 전파전파 합동학술대회

논문집

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장소\_ 한밭대학교

주 최 한국통신학회 마이크로파 및 전파 연구회 전파 엔지니어링랩

후 원\_ (주) 창성, 애드모텍, 에이스테크놀로지, 담스테크, HCT, 맨앤텔

협찬\_ 알트소프트, 이너트론, 에이스웨이브텍



측성 및 물성	좌상 : 김정환 박사 (MCC)	
축물-1	Noise Parameters Measurement Using An 8-Port Network	33
기교 수 16:35-16:50	Abdul-Rahman Ahmed, Kyung-Whan Yeom	
10.55 10.50	Dank Badio Science and Engineering Chungnam National University	
축물-2	개방 단말 Coplanar waveguide를 이용한 유전율 측정에 관한 연구·····	34
16:50-17:05	장지현*, 박래승, 김준환, 박상복, 정용식*, 천창율	
19/20-17/02	서울시립대학교, *광운대학교	
축물-3	무선전력전송용 재구성 공진 코일 연구	35
국물-3 17:05-17:20	이건복, 박위상	
17.03-17.20	교회고기대하고	
축물-4	캐비티 공진기를 이용한 반고체 상태 물질의 복소 비유전을 측정 방법	36
マラマ 17:20-17:35	박래승, 장지현, 김준환, 박상북, 정응식*, 천창율	
17.20-17.55	서울시립대학교, *광운대학교	
	시골시납테시프, 이트레시프	
Session B		
	좌장 : 김흥준 교수 (경북대학	교)
능동부품 1		39
능동-1-1	(초청논문) L-band 마이크로파 라디오미터를 이용한 토양 수분 원격측정 실험	
13:15-13:30	손흥민	
	호남대학교	40
능동-1-2	오남네막교 이중 모드 하이브리드 바이어스 변조기 설계	10
13:30-13:45	정혜련, 함정현, 임원섭, 양영구	
	성균관대학교	
능동-1-3	a - II I chack shad Dower Amplifiers	41
	Linearity improvement for Broadband CMOS stacked Power Amplifiers	
13:45-14:00	With integrated Adaptive bias Circuit	
15.45 14.00	With integrated Adaptive bias Circuit	
20,72	Jaeyong Koo, Dooheon Yang and Sangwook Nam  Sale of Electrical Engineering and INMC Secul National University	42
능동-1-4	With integrated Adaptive bias Circuit	42
20,72	With integrated Adaptive bias Circuit	42
능동-1-4 14:00-14:15	With integrated Adaptive bias Circuit	42
능동-1-4	With integrated Adaptive bias Circuit.  Jaeyong Koo, Dooheon Yang and Sangwook Nam School of Electrical Engineering, and INMC, Seoul National University 고출력, 고효을 특성을 가진 Ku-band GaN 고출력증폭기 집적회로 최윤호, 노윤섭, 염인복 한국전자통신연구원 LHTL형태의 위상변위기를 이용한 광대역 Feedforward Amplifier.	_
능동-1-4 14:00-14:15	With integrated Adaptive bias Circuit.  Jaeyong Koo, Dooheon Yang and Sangwook Nam School of Electrical Engineering, and INMC, Seoul National University 고출력, 고효을 특성을 가진 Ku-band GaN 고출력증폭기 집적회로 최윤호, 노윤섭, 염인복 한국전자통신연구원 LHTL형태의 위상변위기를 이용한 광대역 Feedforward Amplifier 박홍우, 김홍준	_
능동-1-4 14:00-14:15 능동-1-5	With integrated Adaptive bias Circuit	43
능동-1-4 14:00-14:15 능동-1-5	With integrated Adaptive bias Circuit.  Jaeyong Koo, Dooheon Yang and Sangwook Nam School of Electrical Engineering, and INMC, Seoul National University 고출력, 고효을 특성을 가진 Ku-band GaN 고출력증폭기 집적회로 최윤호, 노윤섭, 염인복 한국전자통신연구원 LHTL형태의 위상변위기를 이용한 광대역 Feedforward Amplifier 박홍우, 김홍준 경북대학교 고효율 스위칭 모드 전력증폭기를 위한 6.78 MHz 입력 드라이버 설계	_
능동-1-4 14:00-14:15 능동-1-5 14:15-14:30	With integrated Adaptive bias Circuit	43

## Linearity improvement for Broadband CMOS stacked Power Amplifiers With integrated Adaptive bias Circuit

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#### I. INTRODUCTION

In modern smart handheld devices, there is an explosive demand to handle an increased amount of information and content using the limited available frequency spectrum, such as LTE and worldwide inter-operability for microwave access (WIMAX). Since the modulated signals have high peak-to-average-power ratios (PAPR) with wide bandwidths, PAs should be operated at a back-off power from the peak to satisfy the linearity. Due to the serious level of efficiency degradation from the back-off operation, the linearization technique is crucial at a high power region.

### II. DESIGN AND RESULTS

This paper applies an adaptive bias circuit to the bottom-TR of a stacked PA to improve linearity, using the 0.11-um RF CMOS process. By using the bias circuit, as illustrated in Fig. 1, a sweet spot and peak average output power can be located as a deeper class-AB bias without any linearity distortion at the low-to-mid power region [1]. Considering bandwidth and output power, a stacked topology is employed in this paper and it is composed of four connected transistors in a series, as shown in Fig. 2 [2]. In Fig. 3, the PA with the integrated bias circuit improves 5 dB at the sweet spot of ACLR<sub>E-UTRA</sub>, compared to the constant Class-AB bias PA and shows an average output power of 25.3 dBm, a PAE and DE of 21/29 %, with an ACLR<sub>E-UTRA</sub> of -30 dBc at 1.88 GHz for a LTE 10 MHz 16 QAM 7.5dB PAPR signal. Also, The PA delivers an average output power and

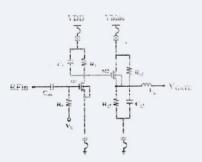


Fig. 1. Schematics of the adaptive bias circuit for the gate of the Bottom-TR

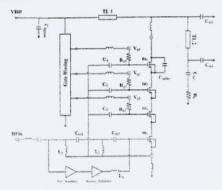


Fig. 2. Overall schematic of broadband 4-stacked PA with the adaptive bias circuit.

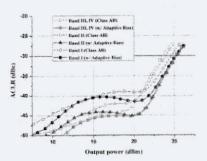


Fig. 3. Measured ACLRs of the designed PA using LTE signal at band I, II, III, and IV.

DE more than 24.5 dBm/25.6 % from 1.55 GHz to 2.05 GHz with the same bias condition. This adaptive bias circuit applied to a stacked PA is useful for broadband linear applications.

#### ACKNOWLEDGEMENT

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- [2] S. Pornpromlikit, J. Jeong, C. D. Presti, A. Scuderi, and P. M. Asbeck, "A watt-level stacked-FET linear power amplifier in silicon-on-insulator CMOS," IEEE Trans. Microw. Theory Tech., vol. 58, no. 1, pp. 57– 64, Jan. 2010.