A Two-Stage Broadband Fully Integrated CMOS Linear Power Amplifier for LTE Applications

Kihyun Kim, Jaeyong Ko, Sungho Lee, and Sangwook Nam, *Senior Member, IEEE*

***Abstract*—This brief presents the implementation and measurement results of a CMOS broadband linear power amplifier (PA) for long-term evolution (LTE) applications. Interstage matching considering the main's source and the driver's load impedances is analyzed for broadband linear output power. The proposed PA is fabricated in standard 0.11-μm RF CMOS technology. The PA achieves linear output power of 27.9–27.3 dBm and power-added efficiency of 33%–26.1% under an adjacent channel power ratio ($\mathrm{ACLR_{E-UTRA}}$) of -30 dBc for an LTE 16-QAM 10-MHz bandwidth signal with a carrier frequency range of 1.8–2.3 GHz.**

***Index Terms*—CMOS power amplifier (PA), full integration, long-term evolution (LTE), transformer, wideband.**

I. Introduction

With mobile communication technologies, such as long-term evolution (LTE) and mobile world-wide interoperability for microwave access (m-WIMAX), a broad-bandwidth power amplifier (PA) is required to keep handset devices small and relatively inexpensive. The CMOS process is suitable for this purpose, although several critical issues, such as a lack of substrate via-holes, a low quality factor, and a low breakdown voltage, can arise. Therefore, many researchers have studied CMOS broadband PAs [1]–[3].

In previous studies, the stacked PA was limited when used to resolve the aforementioned cost and size problems. These PAs use external components for output matching and require a high supply voltage to achieve watt-level output power. Also, the junction diode breakdown problem limits the maximum available supply voltage [4]. For these reasons, the stacked PA is suitable for a floating-body process such as those used with silicon-on-insulator or silicon-on-sapphire processes [5], [6], which are more expensive than standard CMOS processes.

Using a standard CMOS process, a fully integrated transformer-based PA is one of the possible means of solving these issues, i.e., the cost and size problems. This type of PA can achieve watt-level output power by means of power combining based on a transformer without a high supply voltage. Earlier works on mobile applications investigated broadband PAs with a transformer to demonstrate remarkable performance in a PA [1], [7]. However, only single-stage PAs were studied.

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K. Kim, J. Ko, and S. Nam are with the INMC and the School of Electrical Engineering and Computer Science, Seoul National University, Seoul 151-741, South Korea (e-mail: kihyun@ael.snu.ac.kr; sciencedo@ael.snu.ac.kr; snam@snu.ac.kr).

S. Lee is with Korea Electronics Technology Institute, Gyeonggi 463-816, South Korea (e-mail: slee@keti.re.kr).

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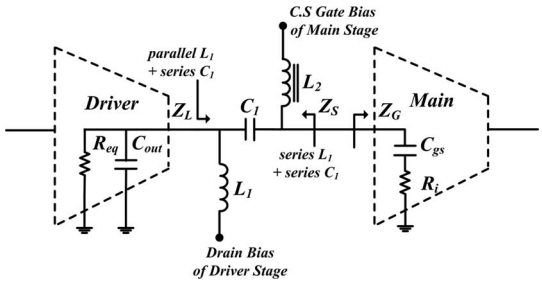

Fig. 1. Interstage matching network for broadband linear output power.

Generally, the bandwidth of the PA according to the maximum linear power is limited by interstage matching between the main and driver stages. This interstage matching changes both the source and load impedance at the main and driver stages. These impedances affect the linearity of the PA across all frequencies [8]. Therefore, interstage matching is a critical issue when designing a fully integrated broadband PA for mobile applications.

In this study, we design and implement a two-stage fully integrated broadband CMOS linear PA using a proposed interstage matching technique. Output matching is implemented by a transformer using the same design topology used in a previous study [9]. The proposed interstage matching is analyzed to determine the degree of linearity across these frequencies. The analysis, based on a two-tone $\mathrm{IMD_3}$ simulation, is explained in detail, and design guidelines are suggested for a broadband linear amplifier. The measurement results of the designed PA using these methods are experimentally demonstrated.

II. Broadband Interstage Matching

Interstage matching between the main and driver stages is very important when designing a broadband linear PA, as the load impedance of the driver amplifier and the source impedance of the main amplifier are determined by the interstage matching. These impedances affect certain performance parameters of the PA, such as the gain, efficiency, and linearity. Therefore, interstage matching should be carefully considered to achieve broadband linearity in a PA.

A two-stage amplifier can be presented as Fig. 1, including interstage matching that is proposed for analyzing the relationship between the source impedances at main stage and third intermodulation ($\mathrm{IMD_3}$). This network minimizes the components for interstage matching and allows for easy control of the impedances related to the main source or driver amplifier.

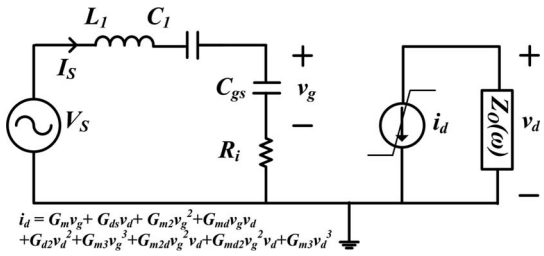

Fig. 2. Thevenin-equivalent circuit at $\boldsymbol{Z_s}$ in Fig. 1.

In addition, $\boldsymbol{R_{eq}}$ and $\boldsymbol{C_{out}}$ are the resistance and capacitance of the output at the driver stage, respectively. Generally, $\boldsymbol{R_{eq}}$ is large enough to be shown as open in a cascode structure if the driver amplifier is operated in a saturation region.

Here, $\boldsymbol{L_1}$ is the load inductor and parallel matching component for the load impedance of the driver, and $\boldsymbol{L_2}$ is the bias inductor of the main stage. It is large enough to be ignored for interstage matching. $\boldsymbol{C_1}$ is a matching component. $\boldsymbol{Z_G}$ is the gate impedance of the main stage, which is presented as a gate-to-source capacitor ($\boldsymbol{C_{gs}}$) and a loss term ($\boldsymbol{R_i}$). $\boldsymbol{L_1}$ and $\boldsymbol{C_1}$ can transfer the main gate impedances to the load impedance for the driver. Simultaneously, these components are shown as a series LC circuit at $\boldsymbol{Z_s}$. Therefore, certain performance metrics of PAs, such as the efficiency, gain, and linearity, can be adjusted by selecting the values of the components $\boldsymbol{L_1}$ and $\boldsymbol{C_1}$.

At the beginning of this section, the effect of source impedance at the main gate is analyzed through the theory and two-tone simulation separated from the driver stage. Then, the two-stage PA including interstage matching is designed with consideration of the driver's load impedance effect.

A. Source Impedance Effect at the Main Stage

Using Thevenin theorem at $\boldsymbol{Z_S}$, the equivalent circuit can be shown as Fig. 2. From a previous analysis of the linearity of a FET [10], the simplified is the IMD$_3$ presented in the following:

$$\begin{aligned}\text{Lower IMD}_3 &= 10\log\left|\frac{P_{\text{IMD}}}{P_{\text{Fund}}}\right| = 20\log\left|\frac{V(2\omega_1-\omega_2)}{V(\omega_c)}\right| - 3\\ &= 20\log\left|\left(\frac{1+G_{ds}}{G_m}\right)V_s^2|r|^2(K_d+K_c)\right| - 3\\ &= 20\log\left|\left(\frac{1+G_{ds}}{G_m}\right)^3\left(\frac{V(\omega_c)}{Z_o(\omega_c)}\right)^2(K_d+K_c)\right| - 3\\ \text{Upper IMD}_3 &= 20\log\left|\left(\frac{1+G_{ds}}{G_m}\right)^3\left(\frac{V(\omega_c)}{Z_o(\omega_c)}\right)^2({K^*}_d+K_c)\right| - 3\end{aligned} \tag{1}$$

where

$$V(\omega_c) = -\frac{G_m Z_o(\omega_c)}{1+G_{\text{ds}}} r V_s \tag{2}$$

$$r = \frac{1}{1+j\omega_c C_{\text{gs}}\left(Z_s(\omega_c)+R_i\right)}. \tag{3}$$

In these equations, $\boldsymbol{P_{IMD}}$ and $\boldsymbol{P_{Fund}}$ are the third intermodulation power level and fundamental power levels at the output, respectively. $\boldsymbol{Z_o(\omega_c)}$ is the effective drain impedance at the carrier frequency, and $\boldsymbol{V_s}$ is the source voltage level related to its input power. $\boldsymbol{K_d}$ and $\boldsymbol{K_c}$ are the complex vectors that are affected by the baseband and second harmonic impedances at the drain node, respectively. $\boldsymbol{Z_s(\omega_c)}$ is the source impedance at the carrier frequency. $\boldsymbol{G_{ds}}$ and $\boldsymbol{G_m}$ are related drain current term defined in [10]. $\boldsymbol{V(\omega_c)}$ is the fundamental output voltage of FET, which can be calculated using a well-known nonlinear current method.

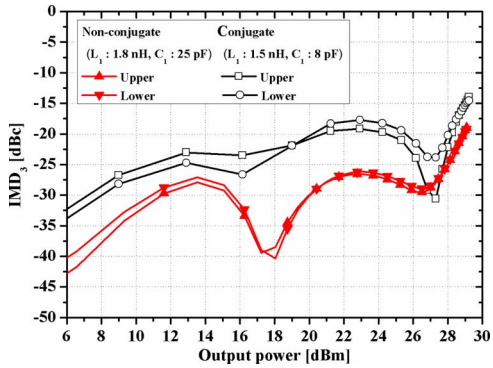

Fig. 3. Two-tone IMD$_3$ simulation results at 1.95 GHz. The results show two cases of conjugate matching and nonconjugate matching at $\boldsymbol{Z_s}$.

To simplify the analysis, if the component for source impedance matching is assumed to be a series inductor $\boldsymbol{L_s}$ and $\boldsymbol{R_i}$ is small enough to be neglected, (3) can be expressed as follows:

$$r \approx \frac{1}{1-\omega_c{}^2 C_{gs} L_s} = \frac{1}{1-\omega_c C_{\text{gs}}\left(\omega_c L_1 - \frac{1}{\omega_c C_1}\right)}. \tag{4}$$

When the denominator of (4) is close to zero, the IMD$_3$ is infinite according to (1) and (2). This result suggests that conjugate matching with the main gate impedance worsens the IMD$_3$. However, (1) and (2) show that the source impedance does not need to be considered to maintain the linearity, when $\boldsymbol{r}$ has a finite value.

The degree of linearity is checked through a two-tone simulation with a 10-MHz tone spacing signal, and the results are analyzed in terms of the source impedance. Fig. 3 shows the IMD$_3$ results of two cases, i.e., conjugate matching and nonconjugate matching at $\boldsymbol{Z_s}$. The values of $\boldsymbol{L_1}$ and $\boldsymbol{C_1}$ for the conjugate matching case are 1.5 nH and 8 pF, respectively. The values of $\boldsymbol{L_1}$ and $\boldsymbol{C_1}$ for nonconjugate matching are correspondingly 1.8 nH and 25 pF. Moreover, the power-added efficiency (PAE) and gain for the two cases are presented in Fig. 4, which shows that gain difference between nonconjugate matching and conjugate matching at the main gate does not exist. It can be verified by calculating the fundamental power gain such as

$$\begin{aligned}\text{Gain} &= 10\log\left|\frac{P_{\text{Fund}}}{P_{In}}\right|\\ &= 10\log\left|\frac{\frac{1}{2}\text{Re}\left(\left|\frac{V(\omega_c)}{Z_o(\omega_c)}\right|^2 Z_o(\omega_c)\right)}{\frac{1}{2}\text{Re}\left(|I_S|^2\left(Z_s(\omega_c)+R_i+\frac{1}{j\omega_c C_{gs}}\right)\right)}\right|\\ &= 10\log\left|\left(\frac{G_m}{\omega_c C_{gs}(1+G_{ds})}\right)^2\frac{\text{Re}\left(Z_o(\omega_c)\right)}{R_i}\right|.\end{aligned} \tag{5}$$

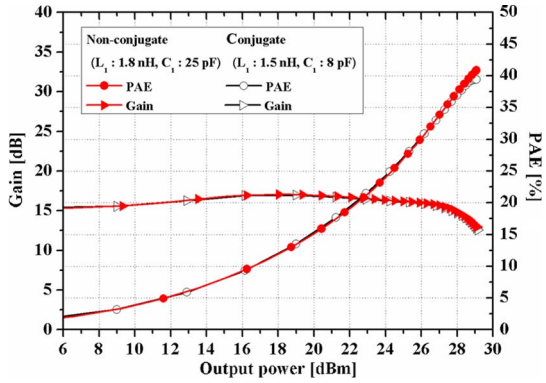

Fig. 4. Gain and PAE achieved by a two-tone simulation at 1.95 GHz. The results show two cases of conjugate matching and nonconjugate matching at $\boldsymbol{Z_s}$.

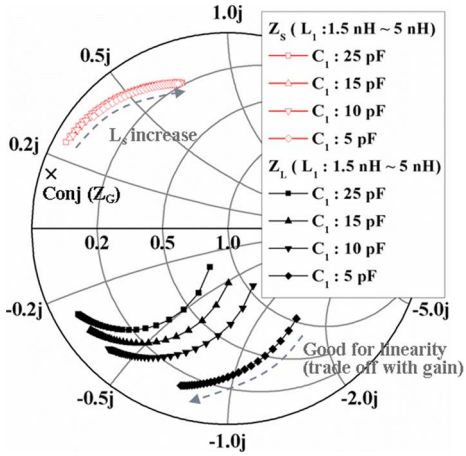

Fig. 5. Load impedance (Z_L) of the driver amplifier and source impedance of the main amplifier (Z_S) to ensure that the maximum linear power exceeds 28 dBm at an IMD_3 level of -25 dBc at 1.95 GHz.

Equation (5) presents that the fundamental power gain is independent on the source impedance of the main stage. The gain is affected by transistor size, frequency, output real impedance, and input parasitic resistance.

These results show that conjugate matching with the gate impedance of the main stage at $\boldsymbol{Z_s}$ should be avoided for good linearity of the PA across operation frequencies. Moreover, the same simulation results can be achieved across 1.8–2.3 GHz.

B. Load Impedance Effect at the Driver Stage

The driver's load impedance affects the total PAE, gain, and linearity of PA. Therefore, the driver's load impedance should be considered with nonconjugate matching at the main gate simultaneously. In this work, the effect of the driver's load in the two-stage amplifier is analyzed through the iterative two-tone simulation by changing the values of $\boldsymbol{L_1}$, $\boldsymbol{C_1}$. Fig. 5 shows the driver's load points $(\boldsymbol{Z_L})$ along with each nonconjugated source impedance points $(\boldsymbol{Z_s})$, respectively. Those points satisfy the maximum linear powers which exceed 28 dBm at a -25 dBc of IMD_3 at 1.95 GHz. The $\boldsymbol{Z_G}$ value is 2.767-j11.126. In addition, IMD_3 is lower than -25 dBc at those points in the output power back-off condition. Among those points, we should find matching point for achieving broadband linearity of the PA.

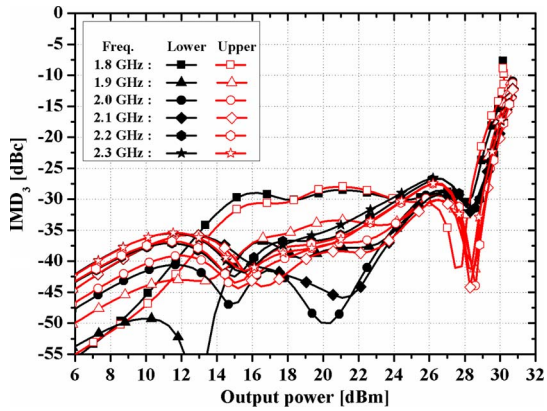

Fig. 6. Two-tone IMD_3 simulation results from 1.8 to 2.3 GHz, when the linear matching points in Fig. 5 are applied at interstage matching.

To ensure broadband amplifier operation, the variation of the driver's load impedance referred to a frequency should be minimized like the load impedance of the main stage [1]. Therefore, the value of $\boldsymbol{C_1}$ is determined as 25 pF for achieving the advantage of the bandwidth. In this case, the driver's load impedance varies along the trajectory of $\boldsymbol{Z_L}$ in Fig. 5 across frequencies.

Then, the efficiency and gain are checked from the results of the simulation at each $\boldsymbol{L_1}$. The driver's load impedance can be changed by varying $\boldsymbol{L_1}$. If the load impedance is to be low, it is the same condition in the back-off operation due to the load line theory [11]. From this reason, the tradeoff between gain, efficiency, and linearity arises at interstage matching. In this work, we limit the minimum gain and efficiency at -25 dBc of IMD_3 to 20 dB and 30% across 1.8–2.3 GHz due to the tradeoff.

Finally, $\boldsymbol{L_1}$ is determined as 1.8 nH through the aforementioned process. $\boldsymbol{L_2}$ is selected for the inductive bias of the main stage and does not affect the interstage matching. The value of $\boldsymbol{L_2}$ is 10 nH, which is feasible for linearity of the PA due to the low impedance at the baseband level. Fig. 6 shows the IMD_3 simulation results of the designed two-stage PA across 1.8–2.3 GHz. The results satisfy the broadband linearity requirement across those frequencies.

III. Implementation and Measurement Results

Fig. 7 shows an overall schematic of the designed two-stage broadband linear CMOS PA, including the interstage matching described in Section II. Symmetry inductors are used for interstage matching and for the main bias. Negative feedback consisting of R_F and C_F is adopted for stability and matching. An on-chip spiral balun is utilized to divide the single-ended input signal into differential signals. A cascode structure is chosen for use with the main and driver stages. The common gate (CG) uses 0.22-μm-thick oxide-type transistors to endure the voltage stress, and the common source (CS) has 0.11-μm-thin oxide-type transistors to ensure a high gain. The total size of the main stage including the CG and the CS is 8.3 mm, and the size of the driver is approximately 1 mm. All bias is provided from the power supply to tune the bias level so as to achieve the best linearity of the PA. The drain supply of the main stage is 3.5 V, and the gate bias of the CG is set to 2.9 V,

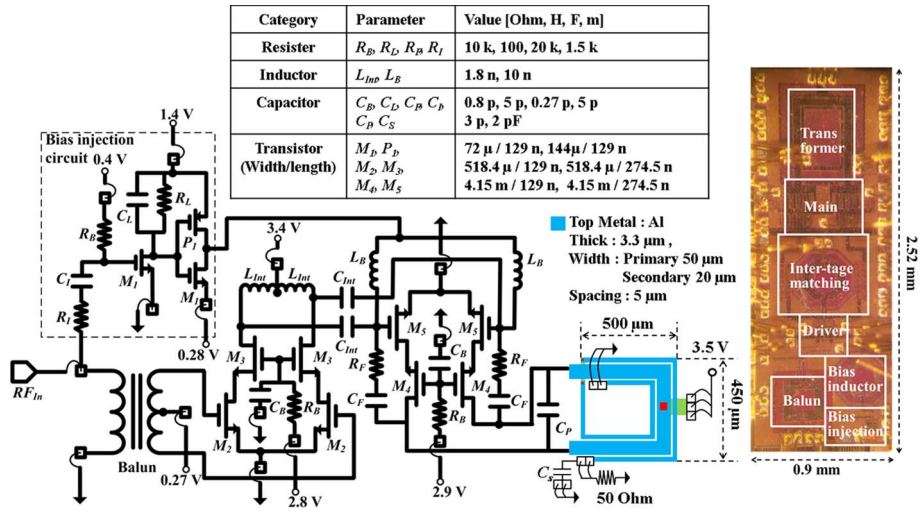

Fig. 7. Schematic of the two-stage fully integrated broadband linear CMOS PA. The geometry of the transformer and a chip photograph are also shown.

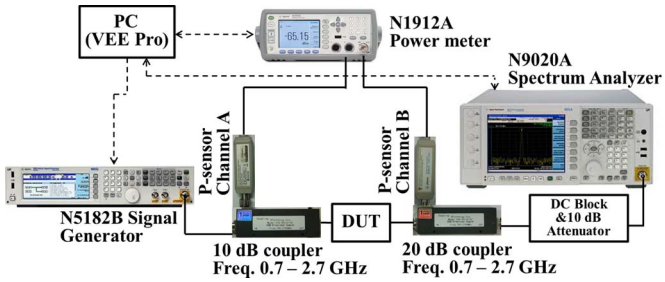

Fig. 8. Measurement setting for the designed PA (DUT) test.

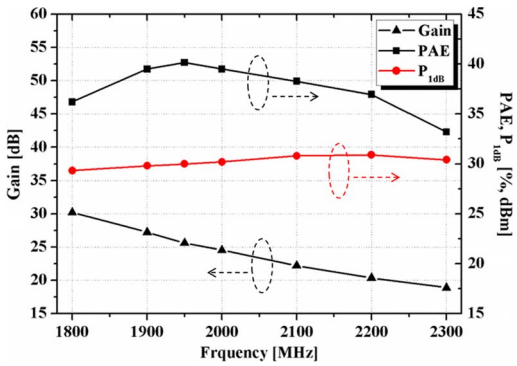

Fig. 9. CW measurement results from 1.8 to 2.3 GHz at a 1-dB compression point.

which is equal to the maximum drain voltage of the CS. For reliability, these bias voltages are verified through dc measurements with power cells. For linearity, a bias injection technique, which was shown to help enhance the linearity and efficiency of a CMOS PA in earlier work [12], is applied to the main stage in this study.

The proposed PA is fabricated via the 0.11-μm 1P8M CMOS process. The process uses 3.3-μm-thick aluminum as a top metal to keep the cost low, although this decreases the quality factor of passive components such as the transformer, balun, and inductor. The total size of the designed PA is 2.52 mm $\times$ 0.9 mm. A photograph of the chip is shown in Fig. 7.

Fig. 8 shows the measurement setting used to verify the performance of the designed PA. The attenuator and couplers

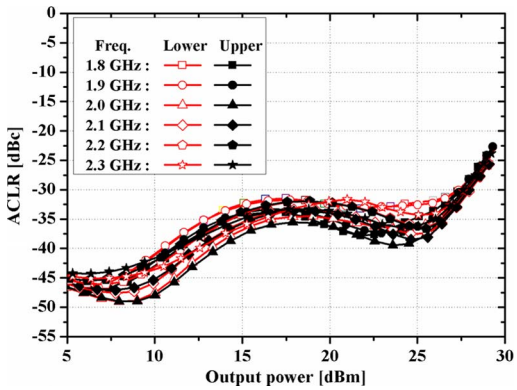

Fig. 10. ACLR measurement results from 1.8 to 2.3 GHz.

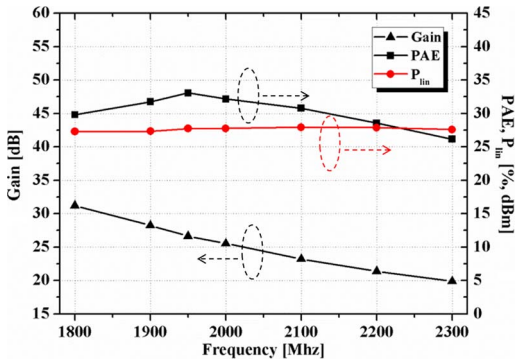

Fig. 11. Measured linear output power at an $ACLR_{E\text{-}UTRA}$ of -30 dBc, with the gain and efficiency from 1.8 to 2.3 GHz.

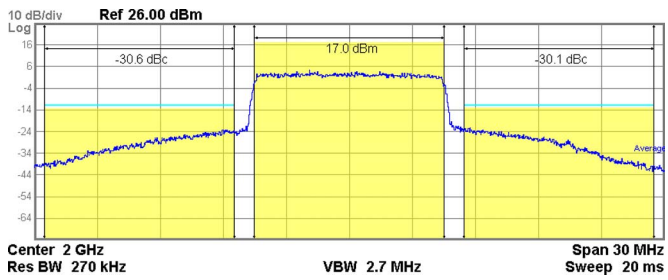

Fig. 12. Output spectrum with 27.76 dBm at 2 GHz.

TABLE I
COMPARISON WITH PREVIOUS WORKS

Ref.	Technology	Structure	VDD [V]	Frequency [Ghz]	[3]P_{OUT} @ ACLR [dBm, dBc]	PAE (%)	Modulation
[2]	0.18-μm SOI CMOS	One-stage differential PA	2.5	1.9 – 2.7	22.4 @ -30	> 18.5	LTE 20 MHz
[1][5]	0.32-μm SOI CMOS	Two-stage stacked PA (Off chip matching)	[2]3.5	0.65 - 1	25 @ -35.5	44 – 38.3	LTE 10 MHz
[6]	0.18-μm CMOS	One-stage differential PA	3.5	1.4 – 2.0	27.5 @ -30.5	36.5 – 31.2	LTE 10 MHz
This work	0.11-μm CMOS	Two-stage fully integrated differential PA	3.4, 3.5	1.8 – 2.3	27.9 @ -30	33 – 26.1	LTE 10 MHz

[1]Muti-chip with a supply modulator
[2]Maximum drain voltage of the PA
[3]Maximum linear output power

protect the test equipment, which is limited in that it has available input power of less than 1 W. For accurate measurements, calibration of the power meter considering the coupling and the insertion loss of the coupler was done from 1.8 to 2.3 GHz. The power meter (N1912A) senses the input and output powers of the device under testing (DUT) through the couplers. A spectrum analyzer (N9020A) is used to measure the $ACLR_{E\text{-}UTRA}$ of the DUT. A 16-QAM 10-MHz LTE or a continuous wave (CW) signal is injected from a signal generator (N5182B). The maximum input power level is adjusted at each frequency due to the gain variation of the DUT. All equipment is controlled by the VEE program for the PC provided by Agilent. The quiescent currents, including the driver and the main stage, are 114 mA due to the class AB bias used for good linearity and efficiency. The CW measurement results from 1.8 to 2.3 GHz are presented in Fig. 9. The PA delivers 1-dB compression output power of 30.9–29.3 dBm with PAE of 33.2–40.1% from 1.8 to 2.3 GHz. To measure the $ACLR_{E\text{-}UTRA}$ of the designed PA, a 16-QAM 10-MHz LTE signal is injected into the PA. Fig. 10 presents the results of the measured $ACLR_{E\text{-}UTRA}$. The linear output power at an $ACLR_{E\text{-}UTRA}$ value of -30 dBc is more than 27.3 dBm from 1.8 to 2.3 GHz. Fig. 11 presents the linear output power with the PAE, showing the gain from 1.8 to 2.3 GHz. The biases of the driver and the main stage are tuned slightly to achieve the highest linear output power. Fig. 12 shows the output spectrum of the designed PA, including the loss of 10.76 dB at 2 GHz. The losses caused by the 10-dB attenuator, the output coupler, the dc-block, and the coaxial cable are shown in Fig. 8.

Table I shows a comparison of the designed PA and a broadband PA described in several publications. The PAE is not good in the comparison with other PAs due to the low-Q on-chip transformer and the power consumption of the driver. However, the designed PA is novel in terms of both its full integration and broadband linear output power for LTE applications.

IV. CONCLUSION

In this brief, we have proposed a two-stage fully integrated broadband linear PA that utilizes load matching with a transformer and interstage matching considering linearity from 1.8 to 2.3 GHz. Although the PAE and some degree of variation of the gain exist at those frequencies, broadband linear output power of the PA is achieved using a broadband matching method which takes into account the degree of linearity. The designed PA shows linear output power of more than 27.3 dBm at an $ACPR_{E\text{-}UTRA}$ value of -30 dBc in a range of 1.8–2.3 GHz, and all PAEs at these frequencies exceed 26.1%.

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