An Integrated Transformer with Reconfigurable S/X-Band Operation in a Single CMOS Power Amplifier

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Abstract **– An integrated reconfigurable transformer for a dual-band power amplifier (PA). The PA operating in the S/X-band is fully integrated using a 0.18-µm RF CMOS process. The switchable transformer is designed by tuning its primary winding and a shunt capacitor at 50 ohm load with passive efficiency of more than 62/67% for S/X-band. The measurement results show saturated output power (P_{SAT}) of 24.3/21.2 dBm with peak drain efficiency (DE) of 34.8%/12.2% at 3.1/8.0 GHz, respectively. The 1-dB bandwidth is 0.7/1.25 GHz (2.8–3.5/7.5–8.75 GHz) for the S/X-band.**

Index Terms **– CMOS, dual-band, power amplifier, radar transceiver, reconfigurable, switch, transformer.**

I. INTRODUCTION

Modern radar systems often require multi-band operations due to the different characteristics of the environment and targets. For examples, S-band signals are resistant to severe weather and atmosphere attenuation. On the other hand, frequencies in X-band are often used for highly resolved target imaging [1], [2]. Achieving dual-band functionality has been challenging, especially when using fully integrated CMOS PAs, owing to their low breakdown voltage and low quality-factor. Most current CMOS PAs are not satisfied by radar systems using the aforementioned frequency bands and several single-band PAs directly assembled into a single chip have been presented [3].

There have been several approaches to implement broadband or multi-band characteristics in a single PA. One approach is to employ a transformer-based high-order output matching network (OMN) or a stacked stepped-impedance transformer to realize wideband operation [4], [5]. However, when using this approach, passive efficiency decreased rapidly, and load matching could not be maintained in lower bands. Another approach is to use parallel/series resonant LC structures or an off-chip combiner [6]; however, these are not suitable for single-chip integration and low-cost implementation.

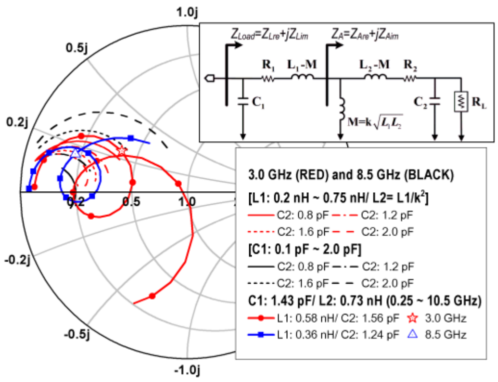


Fig. 1. Normalized Z_{Load} with variations of L_1, L_2, C_1, and C_2 at the S/X-band.

This study proposes a single dual-band PA with a reconfigurable OMN, which is realized through the use of a switchable transformer. The design details and measurement results of the proposed dual-band PA are presented in the following sections.

II. OPERATION OF THE RECONFIGURABLE S/X-BAND PA

A. Reconfigurable Dual-Band Transformer

Given that optimum load resistance (R_{opt}) and device nonlinear output capacitance (C_{device}) in a power device are independent of the operating frequency, the optimum load impedance (Z_{opt}) moves on a conductance circle with $1/R_{opt}$, and smaller shunt inductance is required to resonate with the C_{device} as the frequency increases [7]. As illustrated in Fig. 1, an equivalent circuit of a high-Q transformer and additional capacitors (C_1, C_2) are employed for the OMN. Assuming that the coupling factor (k) is 0.7 and the quality factor (Q) is 10, the transformed impedance was simulated for two cases. First, load impedance (Z_{Load}) was calculated by varying C_1 (0.1~2.0 pF) and C_2 (0.8~2.0 pF), maintaining L_1 (0.36 nH), and optimizing L_2 (0.73 nH) in the X-band. To achieve Z_{opt} for the S-band, the trajectories of

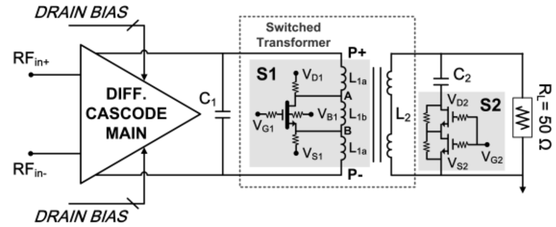
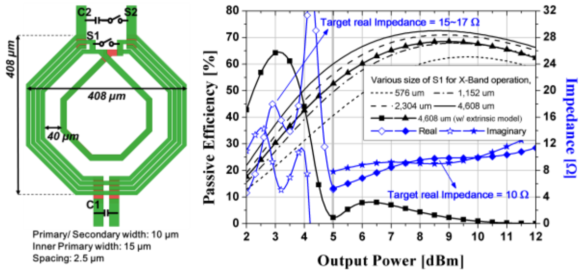


Fig. 2. Schematic of reconfigurable dual-band output matching network with single PA.



(a) (b)

Fig. 3. (a) Physical layout of the OMN, (b) Passive efficiencies with various sizes of S1 and complex impedances for the S/X-band operation.

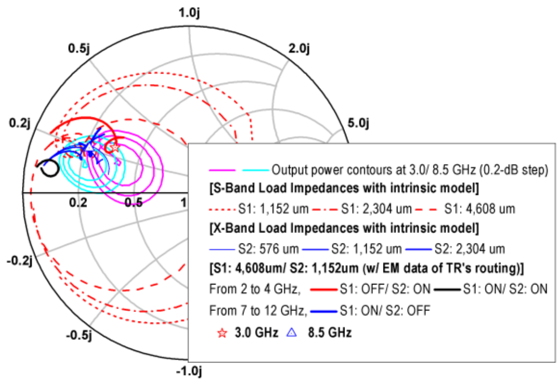
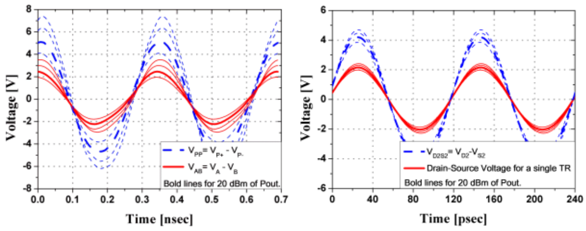


Fig. 4. Normalized Z_{Load} according to various sizes of S1/S2 and different switch operations.

Z_{Load} were drawn by varying L_1 (0.2~0.75 nH) and C_2 (0.8~2.0 pF), and keeping C_1 (1.43 pF) fixed in the S-band. As L_1 increases the real/imaginary parts of Z_{Load} and C_2 precisely controls Z_{Load} to the Z_{opt}, higher L_1 (0.58 nH)/C_2 (1.56 pF) and lower L_1 (0.36 nH)/C_2 (1.24 pF) are required for the S- and X-bands, respectively, with fixed C_1 (1.43 pF) and L_2 (0.73 nH).

The proposed reconfigurable OMN is shown in Figs. 2 and 3 (a); L_1 increases for the S-band due to the inner turn winding and C_2 decreases for the X-band due to the OFF-capacitance (C_{OFF}) of S2. To ensure the operations, S1/S2 is turned OFF/ON for the S-band, while S1/S2 is turned ON/OFF for the X-band. To maintain the high passive efficiency in the X-band, a gap of 40 um exists between the conventional and inner primaries. When considering the gate



(a) (b)

Fig. 5. Simulated voltage difference waveforms: (a) A and B nodes and P+ and P- nodes for S-band operation, and (b) D_2 and S_2 nodes and drain-to-source of a single transistor.

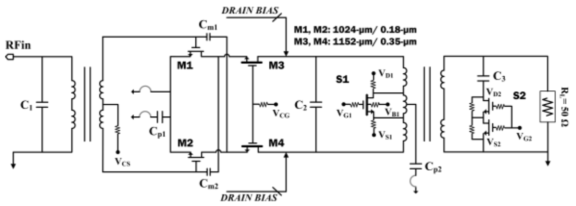


Fig. 6. Schematic of reconfigurable dual-band CMOS PA.

width of S1 for low on-resistance (R_{on}), as shown in Fig. 3 (b), the C_{OFF} must be taken into consideration in order to achieve optimum matching. The trade-off between R_{on} and C_{OFF} results in optimum device widths that balance the effect, as illustrated in Figs. 3 (b) and 4. With a C_{OFF} of 1.69 pF and a R_{on} of 0.9 Ω for the S1, the peak passive efficiencies of the proposed transformer show 64.5%/68.5% in the S/X-band. Including a C_{OFF} of 0.35 pF for the S2, the load impedances at 3.0/8.5 GHz are well located at the targeted impedances (15.5+j15.8 Ω/11.02+j9.54 Ω), as shown in Fig. 4.

B. Circuit schematic of the Dual-Band PA

The S1 (4.608 mm/0.35-μm) and S2 (1.152 mm/0.18-μm) are implemented by a thick gate-oxide transistor and two stacked thin-gate transistors, respectively, which are sufficiently reliable for the OFF-state, as illustrated in Fig. 5. Fig. 6 shows a detailed circuit schematic of the dual-band CMOS PA with the reconfigurable OMN. The designed PA uses two series-resonance circuits for the X-band to alleviate the load asymmetric effects of the OMN, which mainly arise in the practical layout. Furthermore, to the extent that the PA operates stably, Miller capacitors ($C_{m\#}$: 0.25 pF) are utilized to compensate for the gate capacitances of common-source amplifiers. The total gate widths of the common source/gate are

Table 1: Comparison with state of the art CMOS multi-band PAs

Ref.	Freq. [GHz]	Output Network Configuration	OMN Efficiency [%]	P_{SAT} [dBm]	Peak Efficiency [%]	Tech [nm]	VDD [V]	Chip Size/ PA Core Size [mm^2]	PA Type
[4]	5.0/14.0	1 TF +1 inductor (Diff. IN – Single OUT)	[1]30/38	[2]18.5/21.5	[2]6/9.5 (PAE)	90	2.8	0.697/ N.A.	Linear (Class-AB)
[5]	3.5/9.5	1 TF (Single IN – Single OUT)	[3]35/70	[4]19.5/19.0	[4]20/19 (PAE) 24/20 (DE)	40	1.2	1.4/ N.A.	Digital (Class-E)
[8]	1.95/2.4	4 TFs (Single IN – Single OUT)	N.A.	31.8/32.0	28.8/32.4 (PAE)	65	3.6	5.4/ 2.71	Linear
[9]	2.0/6.0	1 TF +3 inductors (Single IN – Single OUT)	N.A.	22.4/20.1	28.4/19 (PAE)	65	3.3	0.89/ 0.68	Linear (Class-AB)
[10]	2.6/4.5	1 TF (Diff. IN – Single OUT)	78.5/62	28.1/26.0	35/21.2 (PAE) 40.7/27 (DE)	65	3.0	2.25/ 0.96	Digital (Class-D^{-1})
This work	**3.1/8.0**	**1 TF +2 SWs (Single IN – Single OUT)**	**64.5/68.2**	**24.3/ 21.2**	**33.4/ 7.7 (PAE) 34.8/ 12.2 (DE)**	**180**	**3.6**	**0.825/ 0.55**	**Linear (Class-AB)**

[1]Values taken from Fig. 10 of [2], [2]Values taken from Fig. 14 of [2], [3]Values taken from Fig. 3 of [3], [4]Values taken from Fig. 5 of [3].

1024/1152 µm with gate length of 0.18/0.35-µm, with a supply of 3.6-V.

III. MEASUREMENT RESULTS

The single S/X-band PA with a reconfigurable transformer is fully implemented in a 0.18-µm 1P6M RF CMOS process that provides a 4.6-µm-thick aluminum layer as the top metal. Occupying a small core area of 0.636×1.297 mm^2 (Fig. 7), the PA is conducive to further

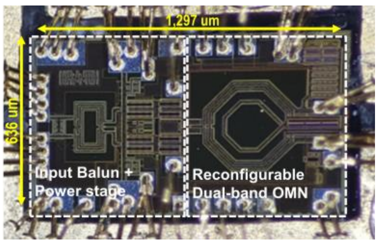
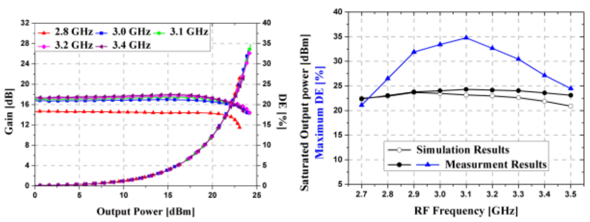
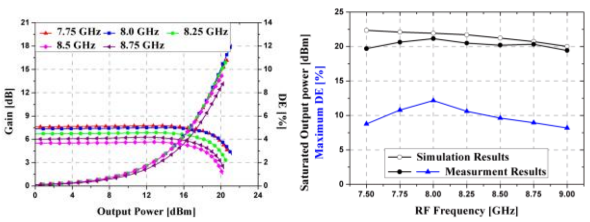


Fig. 7. Microphotograph of PA testing module.



(a) (b)

Fig. 8. Measured gain and DE as a function of output power with CW sources in (a) the S-band and (b) the X-band.



(a) (b)

Fig. 9. Measured P_{SAT} and DE versus frequencies in (a) the S-band and (b) the X-band.

integration with additional transceiver circuits to form a dual-band high resolution radar system on-chip. The IC was mounted on a Duroid 5880 PCB and bond-wire effects are included in the measurement results.

For the S/X-band, the amplifier consumes 222/250 mA of DC current. Figs. 8 and 9 show that P_{SAT} is 24.3/21.2 dBm with peak DE of 34.8%/12.2% at 3.1/8.0 GHz, correspondingly. Note that the discrepancy for center frequencies between the simulation and the measurement is mainly due to large signal modeling of the CMOS and EM modeling. The 1-dB bandwidth is 0.7/1.25 GHz (2.8–3.5 GHz/7.5–8.75 GHz) with P_{SAT} > 23.0/20.0 dBm for the S/X-band, respectively.

IV. CONCLUSION

In this study, a single reconfigurable dual-band PA is fully integrated in 0.18-µm 1P6M RF CMOS technology. This PA consists of a differential power stage with an input/output matching network and operates in the S/X-band. An integrated switchable transformer, a key element of the PA, was studied in terms of the equivalent circuit, the optimum-load matching, and passive efficiencies with transistors as high-power switches. With the OMN passive efficiency being 64.5%/68.2%, the measurement results show that P_{SAT} is 24.3/21.2 dBm and peak DE is 34.8%/12.2% at 3.1/8.0 GHz, respectively. The measured 1-dB bandwidth is 0.7/1.25 GHz (2.8–3.5 GHz/7.5–8.75 GHz) for the S/X-band. Considering the specifications, this PA is likely suitable for use in a dual-band high-resolution radar system.

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