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79 GHz Active Array FMCW Radar System on Low-Cost FR-4 Substrates

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ABSTRACT This work, for the first time to our best knowledge, presents a W-band multi-channel frequency-modulated continuous-wave (FMCW) radar system on low-cost FR-4 substrates. A center-fed patch array antenna on an FR-4 substrate can achieve a maximum gain of 10.8 dBi. It is enabled by aperture coupled feeding using an on-chip feeder implemented on a CMOS radar transmitter (Tx) and receiver (Rx). The proposed radar system consists of one Tx and four Rx channels placed in the back cavity of a microstrip array antenna like an active array antenna system. Additionally, Tx and Rx chipsets include a wideband frequency multiplier with high multiplication ratio of 63, making it easy to distribute reference FMCW waveform synthesized at a very low frequency about 1.25 GHz for 79 GHz output using direct digital synthesis (DDS). Extending the number of channels and implementing various waveforms can be easily accomplished with very good phase noise. The functionality of the proposed radar system on low-cost substrates is confirmed by distance and angle measurements.

INDEX TERMS Multi-channel radar, active array, CMOS, millimeter-wave (mm-wave) packaging, FR-4, high ratio frequency multiplier, on-chip monopole feeder.

I. INTRODUCTION

The use of mm-wave radars for civil and commercial applications has increased due to improvements of low-cost silicon semiconductor technology with mass production capability and good yield. One of the mm-wave radar sensor applications is the advanced driver-assistance system (ADAS) in vehicles. The mm-wave front-end of an ADAS radar sensor requires high performance, high density integration, and low manufacturing cost. Early-stage commercialization of a car radar sensor was initiated by SiGe technology. However, recent market is moving toward CMOS technology that shows a higher level of integration at a more competitive price than SiGe technology [1], [2]. Additionally, CMOS radar transceiver designs are continuously progressing to implement high-resolution imaging radars to support complete autonomous driving [3]. In addition to mm-wave semiconductor technologies, mm-wave packaging technology is also essential for the overall performance, cost, and yield of a product. Traditional metallic packaging composed of waveguides, antennas, and cavities has been an unbeatable solution due to its low-loss nature and high-power

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capability. However, due to its bulky volume, heavy weight, inconvenient interface from chip-to-package, and high manufacturing cost, recent mm-wave packaging for small power applications up to W-band adopts a planar technology utilizing low-loss substrates and flip-chip bonding. Flip-chip bonding for chip-to-board inter-connection shows lower loss and better matching performance than low-cost wire bonding. However, it requires more complicated and expensive processes. Additionally, it is almost impossible to repair a flip-chip bonded system, which could be a problem for massive channel radars. While the mass production capability and continuous scaling of CMOS technology enable gradual cost reduction of active components, the cost for low-loss substrates and its packaging process are marginally decreasing. These packaging issues will become more prominent as the number of radar transceiver channels increases for high resolution.

Compared to a low-loss substrate for mm-wave applications such as liquid-crystal polymers [4], ceramics, and RT/Duriod [5], a low-cost FR-4 substrate has not been an option to implement mm-wave front-end systems. FR-4 substrate has good mechanical and electrical properties. It has been widely used in consumer electronics. However, the loss tangent of FR-4 is about 0.02, which is too high to design mm-wave high gain antennas and low-loss feeding networks. Instead, a modern approach is to laminate low-loss substrates on an FR-4 printed circuit board (PCB). The former is used to form antenna arrays and feeding networks, and the latter is to integrate baseband analog and digital circuits. Even for hybrid stacked PCBs, using a single low-loss layer is preferred in terms of cost and yield [6]. Therefore, recent planar radar systems mount multi-channel transceivers on the same layer on which an antenna array is formed. Therefore, end feeding of series microstrip arrays is unavoidable. When FR-4 substrates are used to implement multi-channel microstrip array antennas, end feeding of series arrays can cause a huge loss due to a long-distance signal distribution network. A 60 GHz mm-wave antenna system on an FR-4 substrate has been proposed in [7]. However, an additional process is required to form the air cavity and a feed line loss is inevitable. A solution to reduce feed line losses on the FR-4 substrate in W-band is to use active antenna arrays [8] where the antenna should be directly fed by active components as close as possible.

This work presents a 79 GHz multi-channel FMCW radar system implemented on FR-4 substrates as shown in Fig. 1. The series patch array antenna on FR-4 substrate is directly fed from the backside through aperture coupling by on-chip feeders on Tx and Rx chips developed in the previous work [5]. These Tx and Rx chips are newly developed for high-ratio frequency multiplication and wideband operation using a 65-nm low-power (LP) RF CMOS process. This paper is organized as follows. Section II describes design details of 79 GHz Tx and Rx chipsets. Section III shows design optimization of center-fed patch antenna arrays and feeding structure on FR-4 substrates. In section IV, implementation of the 1-Tx and 4-Rx FMCW radar system is described. Section V demonstrates measurement results of antenna gain and radar detection capability. Section VI concludes this paper.

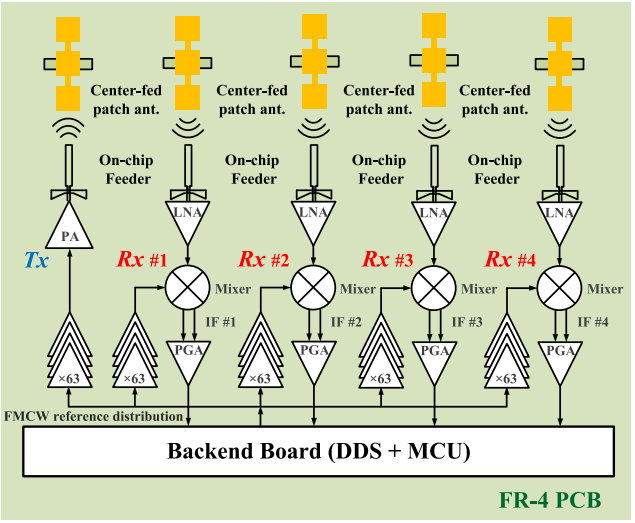

FIGURE 1. Active Array Multi-channel radar structure on FR-4 substrate.

II. CIRCUIT DESIGN

Radar Tx and Rx chips are designed using a 65-nm LP CMOS process with 1-poly 9-metal layers. Their architectures are shown in Fig. 1, similar to those of the previous works [5], [9]. However, all circuit blocks, including a low noise amplifier (LNA), power amplifier (PA), and frequency multiplier, have been newly designed for a wide bandwidth of 5 GHz. Especially, the frequency multiplier has been completely redesigned for low power operation with a high multiplication ratio and a wide bandwidth. Details of each circuit block design are explained in the following.

A. FREQUENCY MULTIPLIER

Since the FMCW reference signal is the highest frequency delivered on FR-4 substrates, its frequency should be made as low as possible for good signal integrity and low power delivery, especially for massive array radars. Theoretically, the first N-push multiplier in the multiplier chain can make any high multiplication ratio. However, practically it is limited due to the reference spur around 79 GHz output, which appears closer and stronger as the multiplication ratio increases. Therefore, a seven-push multiplier is chosen considering the tolerable reference spur. Additionally, since the DDS (Analog devices AD9914) used in this study can generate signals up to 1.4 GHz, the total multiplication ratio should be larger than 58 times to generate a 79 GHz signal output. Therefore, the total multiplication ratio is designed as 63 times using two triplers after a seven-push multiplier. Using DDS instead of phase-locked loops (PLLs) ensures good phase noise and high linearity.

The multiplier chain shown in Fig. 2 is composed of a ring oscillator (OSC) based seven-push multiplier and two

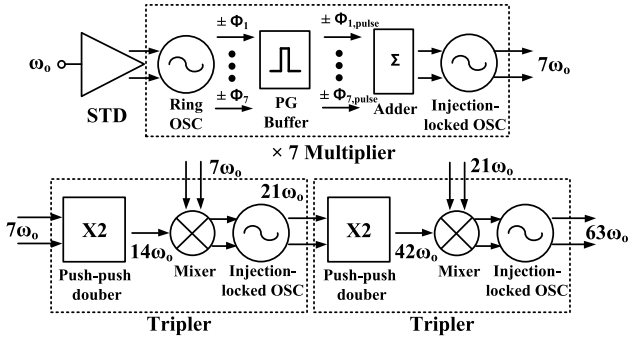

FIGURE 2. Configuration of ×63 frequency multiplier.

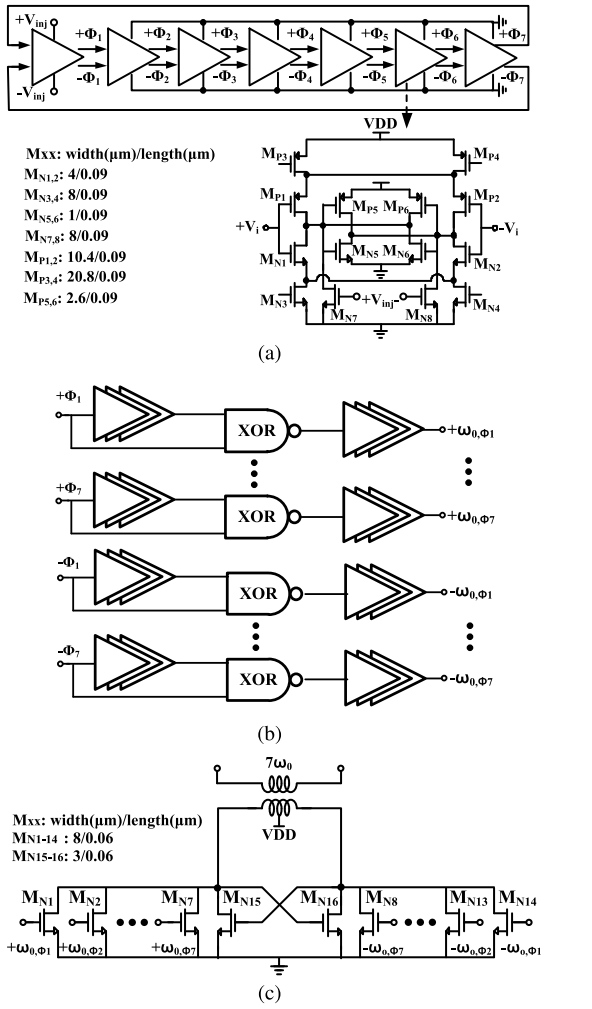

FIGURE 3. Schematic of ×7 frequency multiplier. (a) Seven-phase ring OSC. (b) Pulse generator. (c) Seven-push frequency adder.

mixer-based triplers. Due to the high multiplication ratio amounting to 63 times, the reference input frequency for the final output frequency around 79 GHz is merely about 1.26 GHz. Fig. 3 shows the ×7 multiplier which is composed of a single-to-differential (STD) converter, a seven-phase injection-locked ring OSC with pulse generators, and a seven-push frequency adder. The current starved seven-phase ring OSC is running around 1.26 GHz and locked by an external reference input signal. A single-ended external reference signal is injected through the STD into one of ring OSC cells. Seven differential signals are generated with a phase offset of $2\pi/7$ by these ring cells. If seven-phase signals are ideally combined in the current domain at the adder output, the 7^{th} harmonic and its odd multiples will survive and lower order harmonics are suppressed [10].

Although the operation of the seven-push multiplier is similar to that of the previous work [11], this work newly adds pulse generators to reduce power consumption. In the previous work, the adder was driven by 50% duty pulse directly buffered from the ring OSC [5]. It consumes a lot of currents because every common source (CS) field-effect transistor (FET) in the adder carries the current during the half period of the reference signal with a little phase offset. If narrow pulses drive CS FETs in the adder without signal overlap, the total current consumption is as small as a single CS FET pair of the 50% duty cycle. The pulse is generated using a delay cell and XOR gate. The pulse width is carefully adjusted to maximize the 7^{th} harmonic of the reference frequency. A simple Fourier analysis shows that the optimum delay is half period of the 7^{th} harmonic frequency. The adder output drives the injection-locked OSC to enhance the output signal swing. The negative resistance strength of the OSC is adjusted for the wideband locking range. Simulation results show that current consumption is reduced by 70% compared to the previous work by adopting narrow pulses. Total power consumption of the ×7 multiplier is 22.8 mW from a 1.2V supply.

The next two stages after the ×7 multiplier are mixer based triplers. Fig. 4(a) shows a conventional sub-harmonic mixer-based tripler composed of a switching stage and a frequency doubler at the tail. In a conventional structure, the 3^{rd} order harmonic current at the mixer output gets very small if two input signals V_{11} and V_{12} in Fig. 4(a) are in phase and maximized if the phase difference between two input voltages is around 90° [12], [13]. To enhance the 3^{rd} harmonic output, the conventional mixer based tripler requires a quadrature signal. However, quadrature generation in the mm-wave range requires many resources and becomes more difficult as the frequency gets higher. Therefore, it is not easy to cascade conventional triplers for a high multiplication ratio because both stages require quadrature generation for high output swings. This work separates the frequency doubler as shown in Fig. 4(b) to maximize the 3^{rd} harmonic component without a quadrature signal. The output signal $2\omega_0$ of the separate push-push doubler using M_{N1}, M_{N2} is applied to the transconductance stage M_{N3} of the mixer. According to the previous study [12], the required phase shift in I_{2B} with respect to the phase of the fundamental frequency ω_0 at V_{11} is 180°. In the tripler, due to the transconductance stage M_{N3}, the $2\omega_0$ signal experiences a 180° phase shift in I_{2B}. Fig. 5 shows simulation results of the normalized 3^{rd} order harmonic current of I_{2T} at the mixer output according to the change of phase difference between two input voltages

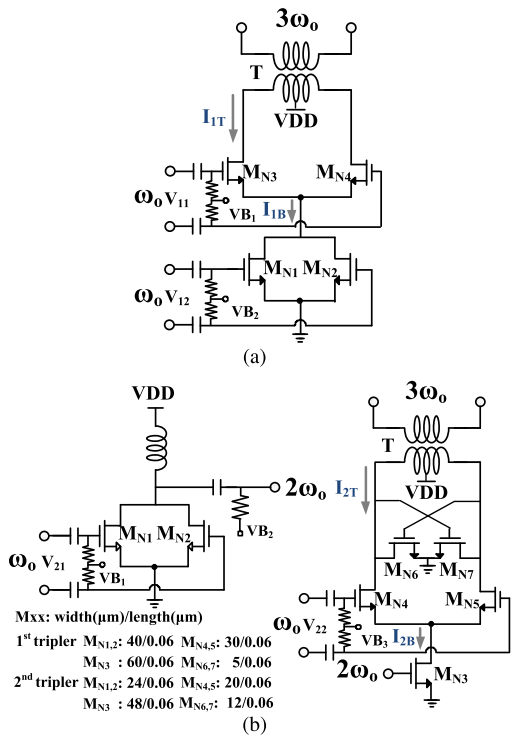

FIGURE 4. Schematic of (a) conventional sub-harmonic mixer tripler. and (b) proposed tripler.

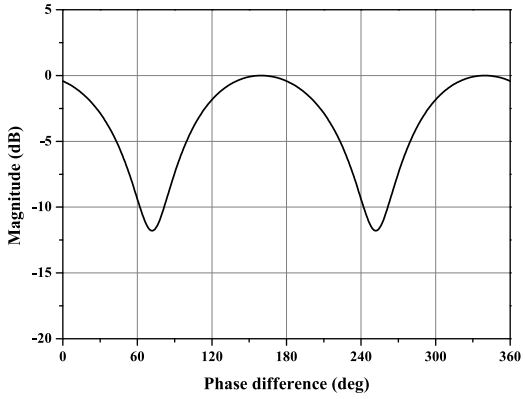

FIGURE 5. Simulation results of normalized 3rd harmonic current at the output of the proposed tripler along phase difference of two input signals.

V_{21} and V_{22} of the second tripler operating with 79 GHz output. As expected, the level of the 3rd harmonic signal is maximized when the phase offset between two input signals is near 0 ° or, 180 ° instead of 90 ° or, 270 ° for the conventional tripler. The injection-locked OSC at the mixer output reduces unwanted harmonic signals and enhances signal swing.

B. TRANSMITTER & RECEIVER

Fig. 6 shows Tx schematic, including the on-chip monopole feeder, which consists of a ×63 frequency multiplier and a three-stage PA. Each stage of the PA has a differential CS amplifier using cross-coupled neutralization to increase gain and stability [14]. For broadband operation, impedance matching at each stage is performed with frequency staggering. Based on the simulations, the peak gain is 15.8 dB and the saturated output power is 11 dBm. The 3 dB bandwidth is from 74 to 83 GHz. Fig. 7 shows Rx schematic including an on-chip monopole feeder. The Rx is composed of a LNA, a single balanced passive mixer, and a ×63 frequency multiplier. The LNA is designed with sufficient gain using four-stage CS amplifiers to suppress flicker noise of the mixer and baseband circuits. Similar to PA, a cross-coupled neutralization technique is used to increase gain and stability. Impedance matching of the LNA uses a concentric transformer and a balancing capacitor (C_1, C_2) at the input and output to suppress the common mode. A differential common-gate amplifier using pMOS FETs is used to ensure low input impedance for the operation of the current mode mixer. Die micrographs of fabricated Tx and Rx chips are shown in Fig. 8. Chip sizes of Tx and Rx are 0.8 mm × 2.4 mm and 0.9 mm × 2.5 mm, respectively.

C. TX AND RX MEASUREMENT RESULTS

Tx and Rx chips with RF pads were fabricated separately to evaluate chip performance using on-wafer probing. A reference input signal of 0 dBm from the signal generator (Keysight N5173B) is applied to the multiplier input of Tx and Rx chips. Fig. 9 shows simulation and on-wafer measurement results of the Tx output power. The measured maximum output power is 10.93 dBm at 78.75 GHz. The output power above 10 dBm is observed in the frequency-locked range from 77 GHz to 82 GHz. As shown in Fig. 10, phase noise of the 78.75 GHz Tx output is -97.91 dBc/Hz at 1 MHz offset for the reference signal of 1.25 GHz with -135.89 dBc/Hz phase noise at the same offset. The phase noise degradation is 37.98 dB, which is close to the amount of the theoretical degradation of 35.9 dB. Spurs of the output signal were investigated with a PXA signal analyzer (Keysight N9030A) and a W-band harmonic mixer (Keysight 11970W). Spurious tones around the 79 GHz output signal exist with a tone spacing of the reference frequency, but the reference spur suppression is more than 30 dBc. The DC power consumption of the Tx is 217 mW.

The conversion gain of the Rx chip was measured by applying W-band signal available from a vector network analyzer (VNA: Anritsu MS4647A, 7379B). IF signal output was analyzed using a spectrum analyzer. As shown in Fig. 11, the conversion gain has a peak of 30.1 dB at 78.75 GHz and a 3 dB bandwidth of 77.5 to 82 GHz. Rx noise figure (NF) was roughly estimated using the spectrum analyzer as in the previous work [5]. The measured NF is 13 dB at 1 MHz IF signal. The DC power consumption of the single-channel Rx is 154 mW from a 1.2 V supply.

III. SLOT COUPLED SERIES MICROSTRIP ARRAY ANTENNA ON FR-4 SUBSTRATE

In this work, an aperture coupled microstrip array antenna is implemented on FR-4 substrates, where the center patch is fed

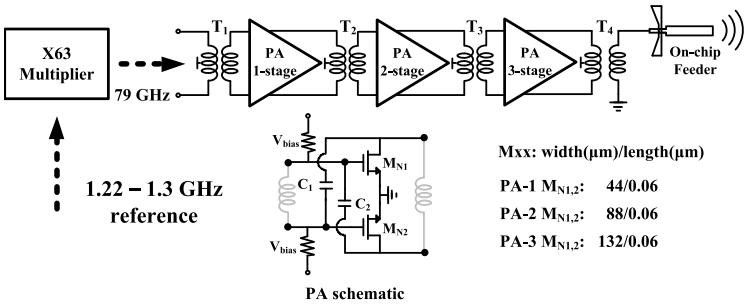

FIGURE 6. Frequency multiplier-based Tx.

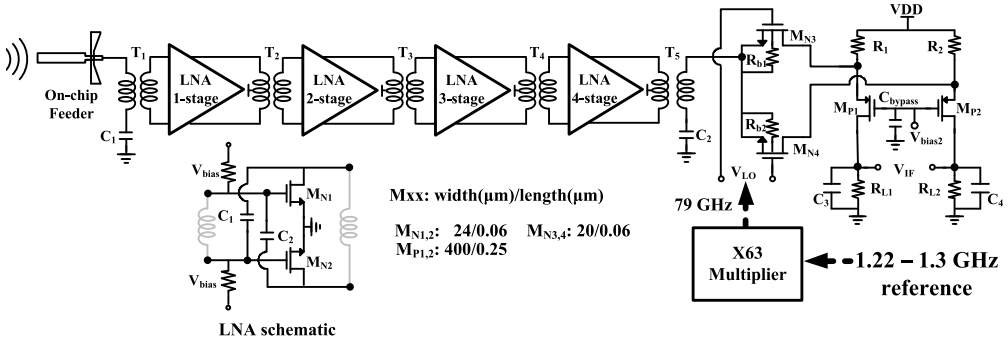

FIGURE 7. Frequency multiplier-based Rx.

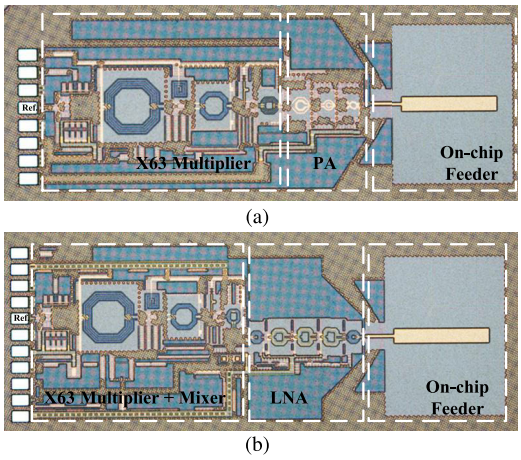

FIGURE 8. Die micrograph (a) Tx chip. (b) Rx chip.

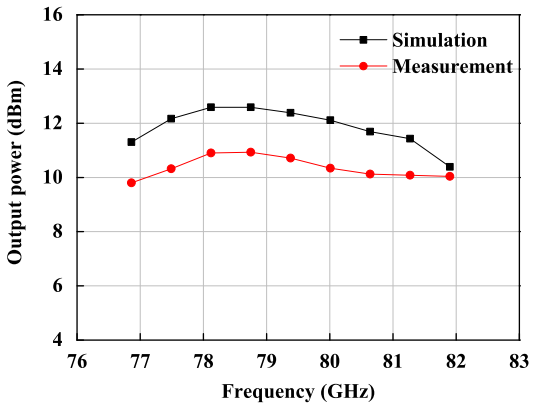

FIGURE 9. Tx output power simulation and measurement results.

by an on-chip feeder on a silicon chip as shown in Fig. 12. The on-chip feeder in Fig. 12 was originally developed for vertical interconnect from the silicon chip to the transmission line on RT/Duriod 5880 without using conductive bonding techniques or thru vias. The center patch of the microstrip array is driven through the slot which is formed on the back-side ground plane of the microstrip array as shown in Fig. 13. By attaching Tx or Rx chip directly to the center slot of each array, a long feeding network can be eliminated to avoid huge losses of FR-4 substrates.

In Fig. 13, the microstrip antenna array is composed of the center patch fed by slot and the off-center patches fed by half wave-length transmission line in up and down directions. To maximize the gain of the array in the lossy FR-4 substrate, the thickness of the substrate, and the characteristic impedance of the transmission line section are carefully determined considering the line loss, the element gain and manufacturability.

First, the transmission line section is simulated using ANSYS HFSS to examine attenuation characteristics of transmission lines depending on the thickness of FR-4 substrate. Since the available thickness of the FR-4 substrate from a standard low-cost PCB process is limited to 0.2 mm, three different thicknesses having the multiple of 0.2 mm are evaluated. Simulation results are summarized in Table 1

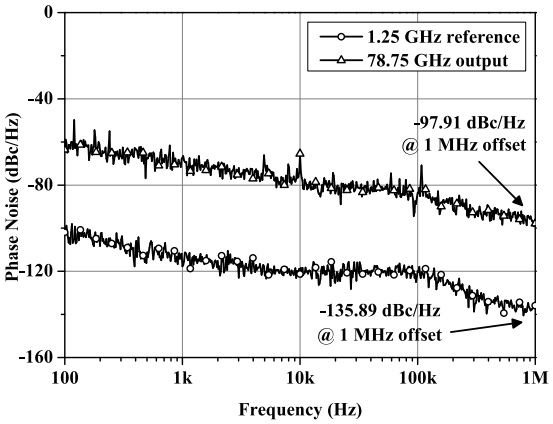

FIGURE 10. Tx phase noise measurement results.

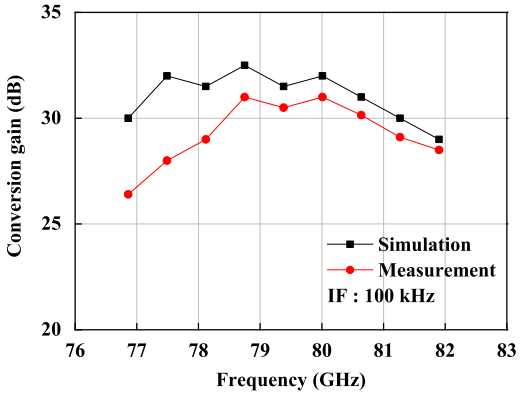

FIGURE 11. Rx conversion gain simulation and measurement results.

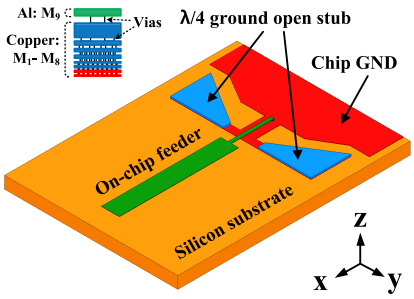

FIGURE 12. Structure of the on-chip feeder and ground open stub on a silicon substrate [5].

TABLE 1. Insertion loss variation of microstrip line with respect to the characteristic impedance and FR-4 substrate thickness.

Thickness	50-Ω Line		110-Ω Line	
(mm)	Loss (dB/mm)	Width (mm)	Loss (dB/mm)	Width (mm)
0.2	0.25	0.3	0.22	0.05
0.4	0.28	0.7	0.25	0.12
0.6	0.3	1.08	0.3	0.19

and the high impedance line on the thinner substrate showed less loss. The overall gain of the center-fed array antenna is determined by combining the gain of the series patch and the

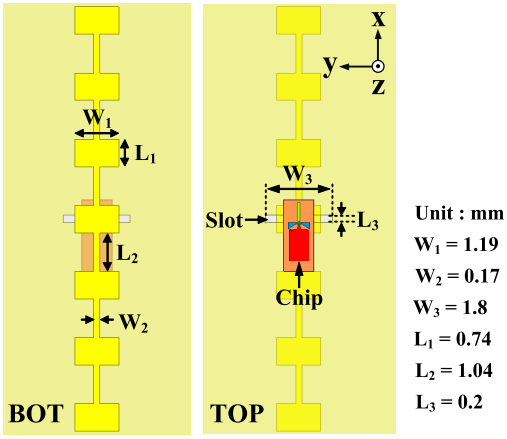

FIGURE 13. Top and bottom views of the microstrip patch array antenna center-fed by an on-chip feeder with dimensions.

TABLE 2. Gain change of single patch antenna with respect to feeding method and FR-4 substrate thickness.

Thickness (mm)	Slot fed patch gain (dBi)	Edge-fed patch gain (dBi)
0.2	3.33	3.02
0.4	3.88	2.37
0.6	-1.4	1.95

center patch antennas. Table 2 shows gain change of the slot coupled center patch antenna fed by the on-chip feeder and the edge-fed patch antenna with a λ/2 transmission line in the series array according to the thickness of the substrate. It is found in the simulation that the gain and pattern of the single patch antenna show large variations depending on the size of the ground plane and the thickness. In particular, for the edge-fed patch antenna, the elevation pattern is greatly affected by the length of the ground plane due to the surface wave mode. It is known that an FR-4 substrate with a high thickness and dielectric constant is very vulnerable to surface wave mode generation [15]. Therefore, when evaluating single antenna gain for comparison as shown in Table 2, the size of the ground plane is optimized for the best gain. According to simulation results, a thinner substrate is better for high gain patch antenna suppressing the surface wave mode. However, as seen in Table 2 and Fig. 14, the center patch antenna fed by the slot shows better gain with the substrate of 0.4 mm thickness than 0.2 mm thickness. It is very beneficial for overall gain because the series edge-fed patch antennas suffer from severe attenuation along feeding transmission lines. Additionally, since Tx and Rx chips are directly attached to the antenna ground plane, mechanical rigidness is also important. Therefore, the substrate with thickness of 0.4 mm was used to form the antenna array. Fig. 15 shows the gain of the center fed series array with the number of patch array elements on the FR-4 substrate with 0.4 mm thickness and it is found that the antenna gain of the array with more than seven elements does not increase due to feeding line losses.

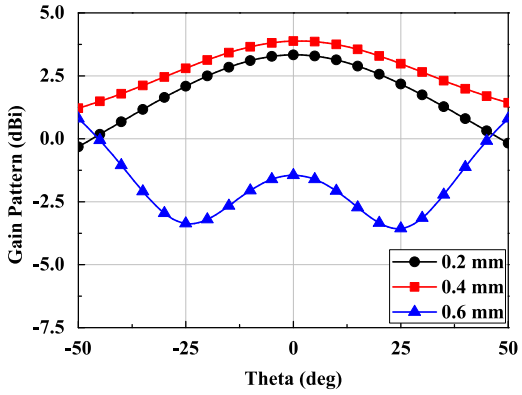

FIGURE 14. Simulation results of antenna radiation pattern of slot coupled single patch antenna according to FR-4 substrate's thickness.

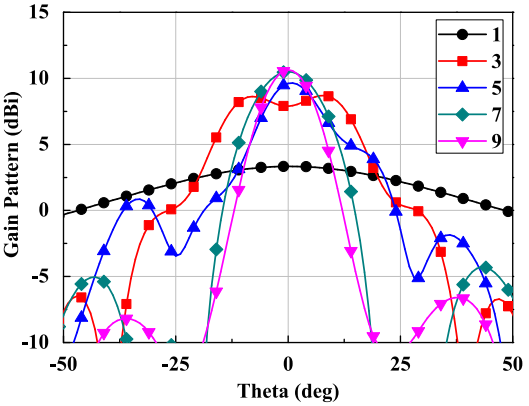

FIGURE 15. Simulation results of antenna gain with the number of patch array elements on the FR-4 substrate with 0.4 mm thickness.

The benefit of a center-fed patch array is that the degradation of the elevation pattern due to the surface wave mode is marginal because it is gradually and symmetrically attenuated along the axis of the antenna. Therefore, edge diffraction at the antenna boundary is negligible. Additionally, the center-fed array antenna is beneficial for a wideband system because the end feeding of the series array is annoyed by the gradual beam tilting as frequency changes. While the center feeding using transmission lines requires an additional 180° phase shifting section [16] or coupled line sections [15] for differential mode antenna operation, the aperture coupling beneath the center patch can inherently feed the series array in a differential mode. Fig. 16 shows E-field distribution at radiating edges of the slot coupled center patch antenna. It confirms that E-field distribution is successfully phase-reversed to feed upper and lower series arrays in a differential mode.

IV. PACKAGING AND INTEGRATION OF MULTI-CHANNEL RADAR SYSTEM

This section discusses the implementation of a multi-channel radar system on FR-4 substrates. An exploded view of the radar RF board is shown in Fig. 17. The radar RF board

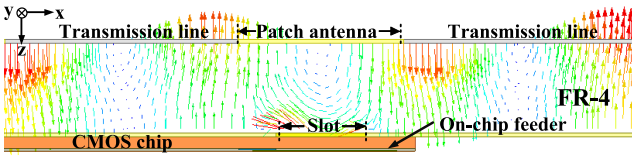

FIGURE 16. EM simulation results of E-filed distribution near the edges of the center patch antenna.

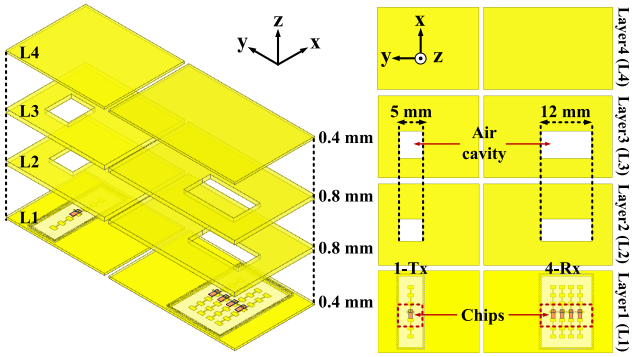

FIGURE 17. Exploded view and detailed description of the proposed radar board packaging.

uses four layers of FR-4 substrates. The patch array antenna designed in Section III is formed on the bottom side of the L1 layer, which is the lowest substrate in Fig. 17. As discussed in [9], Tx and Rx chips are thinned to 50 μm to lower substrate losses. They are mounted on the top surface of the L1 layer aligned with slots, which are formed on the ground plane of the center patch of the series array. Attaching chips to slots, alignment between the ground open stub and the slot should be controlled within 50 μm to keep gain degradation less than 0.2 dB. The second layer L2 is the interfacing layer with two rectangular holes in which 1-Tx and 4-Rx chips are placed. Chip pads are ball-bonded to bonding pads on the top surface of the L2 layer which is closely placed to the sidewall of rectangular holes. Pads on the L2 layer are interconnected to subsequent baseband circuit blocks such as programmable gain amplifiers (PGAs), bias lines, and the reference LO signal.

In addition, the L2 layer forms the back cavity for Tx and Rx chips together with the L3 and L4 layers to suppress backlobes and encapsulate chips for protection. The L3 layer has longer rectangular holes than the L2 layer to secure the space for bonding wires and their landing spots in the L2 layer. When the on-chip feeder feeds the waveguide, the short plane of the back cavity is placed at a quarter-wave distance about 1 mm to reflect the backward wave [9]. However, in the proposed planar integration, the field from the feeder is tightly coupled to the FR-4 substrate underneath the slot due to its high dielectric constant. Therefore, unlike waveguide applications, input matching is not so sensitive to the height of the back cavity. Simulation results for various heights from 0.4 mm to 1.6 mm of the back cavity show little change of input matching. The total thickness of the L2 and L3 layers is determined to be 1.6 mm safely considering the

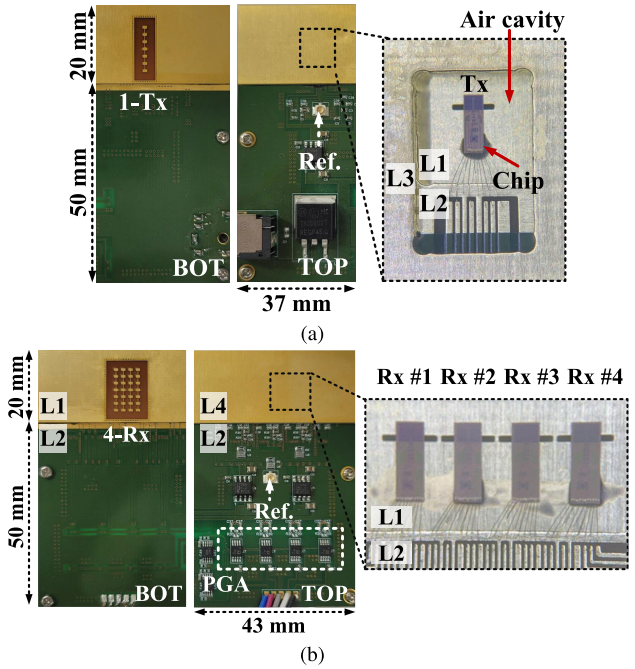

FIGURE 18. Top and bottom view of the radar board. (a) 1-Tx. (b) 4-Rx.

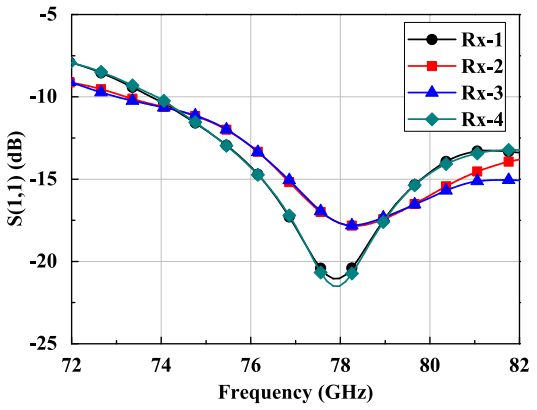

FIGURE 19. Simulated return losses of the transition from on-chip feeders to center-fed patch antennas.

height of bonding wires, but it can be reduced even less than a quarter-wave length if low profile bonding techniques are available.

Internal sidewalls of these rectangular holes in L2 and L3 layers and both sides of the L4 layer are gold-plated to electrically shield the cavities for Tx and Rx chips. The spacing between 4-Rx's is λ/2. Tx and Rx antennas are separated as far as 9.5λ with guard vias to reduce interference from the Tx to the Rx generated by surface wave modes. Thicknesses of FR-4 substrates are 0.4 mm, 0.8 mm, 0.8 mm, and 0.4 mm for L1, L2, L3, and L4 layers, respectively. These FR-4 substrates are laminated using non-conductive epoxy (STYCAST A312-20). Fig. 18 shows the manufactured 1-Tx in (a) and 4-Rx radar board in (b).

Fig. 19 shows simulation results of return losses seen from the feeding point of on-chip feeders of Rx chips in the cavity

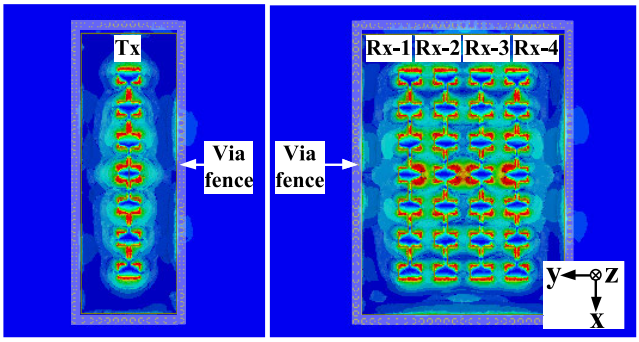

FIGURE 20. E-field distribution in the RF radar board.

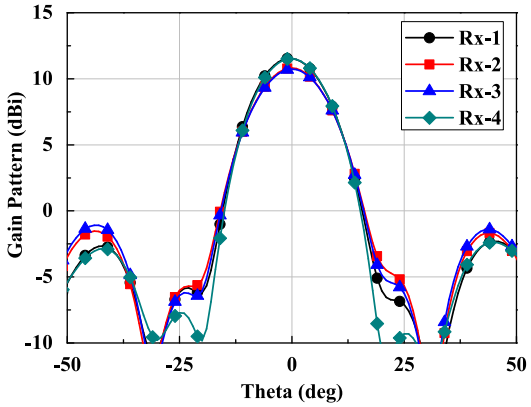

FIGURE 21. Antenna gain pattern simulation results for each Rx channel.

of the radar board. It is confirmed that most of the signal from the on-chip feeder around 79 GHz is transferred to the antenna array on the board. Asymmetry of return losses between Rx-1,4 and Rx-2,3 seems to be due to different boundary conditions for surface wave modes. In addition, isolation between 4-Rx channels is better than 30 dB based on simulation results.

Fig. 20 shows E-field distribution on the FR-4 radar and the surface wave mode is found along the H-plane in the FR-4 substrate. However, it is effectively suppressed beyond surrounding vias. Mutual coupling between Tx and Rx is negligible. Based on simulation results, the isolation between the Tx and Rx's is better than 100 dB at 79 GHz, which is sufficient to prevent Tx leakage to Rx.

Fig. 21 is the antenna gain simulation results of 4-Rx channels. Due to asymmetric boundaries seen from each antenna and surface wave modes, gains and sidelobe levels of four receiving channel are slightly different. However, the main lobe gain shows variations less than 1 dB and the overall performance of the radar system is not severely deteriorated.

Fig. 22 shows the backend board that contains a micro-controller unit (MCU: STM 32F303RE), a DDS, a PLL, and a voltage-controlled oscillator (VCO). The DDS generates various modulated waveforms below 1.4 GHz for a system clock of 3.5 GHz. The DDS system clock is made using PLL (Analog devices AD4159) and VCO (Crystek CVCO55CCQ-3500-3500). Since the DDS output has many unwanted spurs, a band-pass filter (Mini circuit

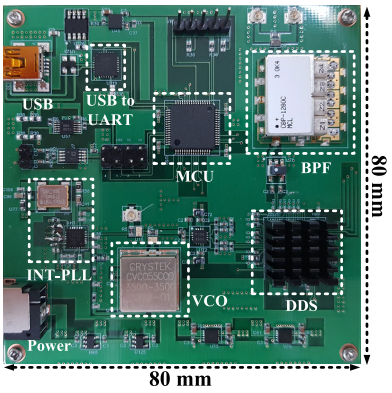

FIGURE 22. Configuration of the backend board.

ZX75BP-1250+) is used to suppress these spurs. The MCU controls the DDS and PLL and samples IF data using internal 4-channel ADCs.

V. RADAR MEASUREMENT RESULTS

A. ANTENNA PATTERN MEASUREMENT RESULTS

Fig. 23(a) shows a setup for gain measurements. The setup has transmitting and receiving antennas and a rotating positioner. A comparison method is used to determine the gain of the proposed center-fed microstrip array antenna of the Tx on the radar board. The receiving antenna is a standard horn antenna with a 24 dBi gain. Received power is measured using a W-band harmonic mixer and a spectrum analyzer. The aperture plane of the receiving antenna is 75 cm away from the transmitting antenna mounted on the rotating positioner with $\pm 50^\circ$ change. At first, another standard horn antenna is placed at the transmitting position. It is driven by the known output power at 79 GHz available from the VNA output. The received power is recorded and verified using the Friis transmission equation. Then, the developed radar board is mounted on the transmitting position and driven by the fixed LO reference frequency for 79 GHz output. The transmitting power from the Tx chip is assumed to have the same value as the measured one shown in Fig. 9. The received power from the radar transmitter is measured and compared to that of the standard horn antenna. Figs. 23(b) and 23(c) show simulated and measured results of E- and H-plane patterns of the proposed FR-4 antennas. The measured maximum gain is 10.8 dBi and the 3 dB beamwidth is $\pm 20^\circ$ azimuth and $\pm 5^\circ$ elevation. It can be seen that the measured pattern at 79 GHz closely matches the simulated one. The back lobe was also measured after flipping the radar module. The measured front-to-back ratio (FBR) is 34 dB, which is similar to the simulated value of 35 dB. Compared to the previous work without a back cavity [5], the FBR is improved by approximately 23 dB. A performance comparison with published mm-wave radar systems is shown in Table 3.

B. DISTANCE MEASUREMENT RESULTS

FMCW radar operation was measured using a 500 μs triangular waveform from 80.64 to 81.9 GHz by activating the DDS.

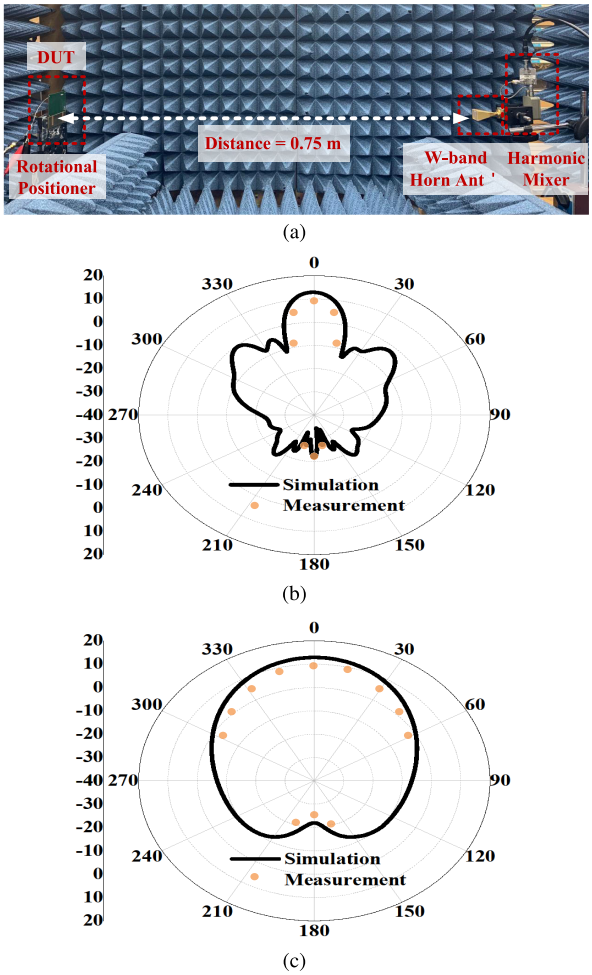

FIGURE 23. Simulated and measured gain patterns of the integrated Tx module at 79 GHz. (a) Antenna pattern measurement setup. (b) E-plane gain. (c) H-plane gain.

Fig. 24(a) shows an outdoor measurement setup for range detection. The proposed radar system was installed at a height of 80 cm from the ground and a trihedral corner reflector (SAGE Millimeter SAJ-043-S1) with a radar cross-section of 10.4 dBsm at 80 GHz was used as a target. Fig. 24(b) shows echo signals from the target and environment clutters. The target was identified by moving its location and observing the corresponding change of the IF frequency. The target at 30 m away from the radar was detected at 1008 kHz IF frequency with an SNR of 16 dB. The maximum gain variation between the channels was observed to be about 3 dB. This received power is reasonably similar to the calculated one taking into account the Rx gain of 28 dB, the Tx power of about 10 dBm, the PGA gain of 20 dB, and the antenna gain of 10.8 dBi using the radar equation [21]. The roll-off of the noise floor spectrum around dc was due to characteristics of the DC block.

C. ANGLE MEASUREMENT RESULTS

The direction of arrival (DOA) can be estimated using four-channel received data. To evaluate the angle detection

TABLE 3. Comparison of some mm-wave radar systems.

Source	[17]	[5]	[18]	[19]	[1], [20]	This work
Technology	130-nm SiGe	65-nm CMOS	MMICs	65-nm CMOS	45-nm CMOS	65-nm CMOS
Frequency (GHz)	60	77	77	77	77	77
Measurement bandwidth (GHz)	3	0.56	2	4	4	5
#Tx/#Rx	4/8	1/1	6/8	2/3	3/4	1/4
Phase noise @ 1 MHz offset (dBc/Hz)	N/A	-103.6	N/A	-87.4	-94	-99
Tx output power (dBm)	7	9	10	13.4	10.8	10
Rx conversion gain (dB)	18	34	15	26.2 to 78.8	N/A	27
Rx NF (dB)	6.3 @ 1 MHz	12.7 @ 1 MHz	N/A	15.3 @ 600 kHz	18 @ 1 MHz	13 @ 1 MHz
Antenna substrate	Astra MT77	RT/Duroid 5880	TLE-95	RO3003	RO4835	FR-4
Antenna gain (dBi)	12	11.8	10	11.2	11.7	10.8

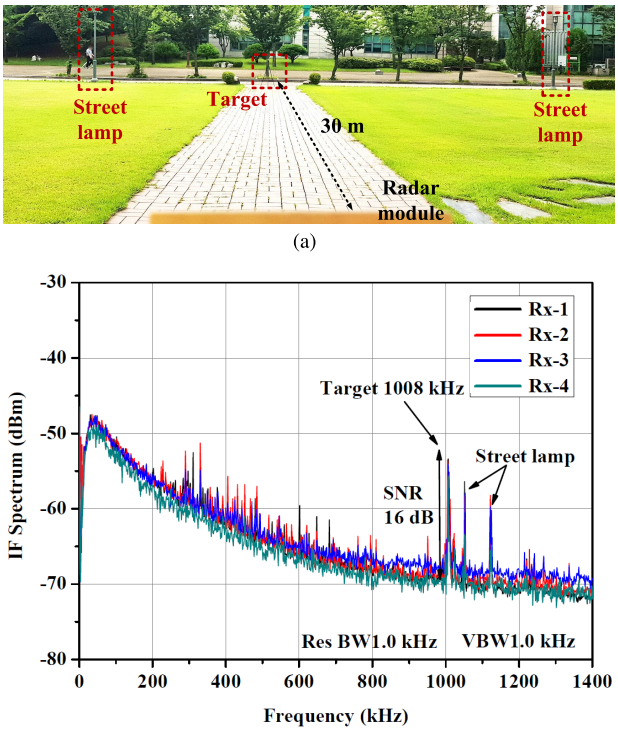

FIGURE 24. Range measurement results. (a) Distance measurement setup. (b) IF spectrum results.

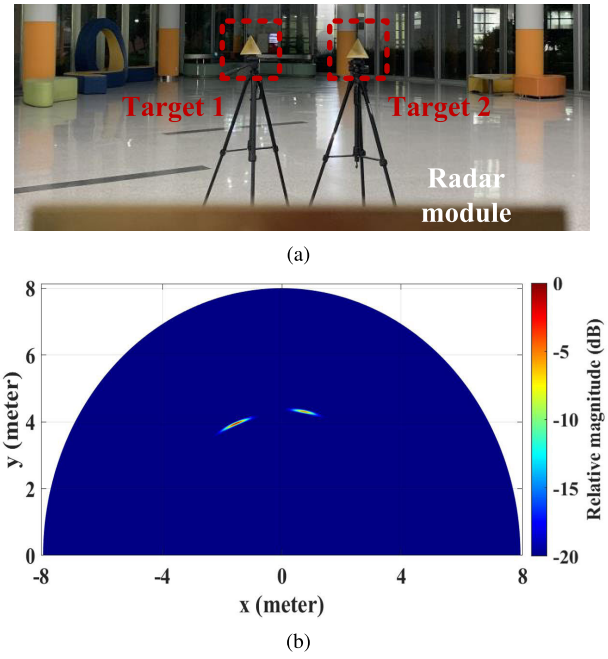

FIGURE 25. Angle measurement results. (a) Angle measurement setup. (b) DOA measurement results.

capability of the proposed radar system, the conventional delay and sum beamforming algorithm was adopted [22]. Beam steering is effective on the premise that IF signals of the four receiving channels have the same phase of the target located at an angle of 0 °. In the proposed active array system, accurate phase synchronization between Rx channels is not easy at the design time because the FMCW reference signal distribution at the board level cannot be accurately controlled due to tolerances in PCB manufacturing. Therefore, the phase of received signals is not identical, mainly due to different delays in the reference LO distribution network from the DDS. To calibrate the phase offset for each channel, a reference target positioned at the right front of the radar was measured. Fig. 25 shows the measurement setup and DOA measurement results of two targets. These results were obtained by moving the beam steering vector by ±90 ° in 1 ° step.

VI. CONCLUSION

This work implemented a 1-Tx, 4-Rx 79 GHz FMCW CMOS radar system on a low-cost FR-4 board. The FR-4 board is cost effective with good manufacturability. However, the high loss from the chip to the antenna array and the low efficiency of the antenna make it difficult to implement a W-band system on the FR-4 board. This work overcomes performance degradation of the FR-4 board in the W-band by feeding a separate antenna directly from a chip equipped with an on-chip feeder like an active antenna system. The integrated patch antenna on the FR-4 substrate was found to have a gain more than 10 dBi. The fully integrated 4 channel Rx array was evaluated by range and DOA detection. Since the number of channels

can be easily expanded, the proposed low-cost system could be a cost-saving solution for a high-resolution radar.

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REFERENCES

[1] B. P. Ginsburg *et al.*, "A multimode 76-to-81GHz automotive radar transceiver with autonomous monitoring," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 158–160.
[2] *MR3003 High-Performance 77 GHz Radar Transceiver*. Accessed: Sep. 5, 2020. [Online]. Available: https://www.nxp.com/products/rf/radar-transceivers/mr3003-high-performance-77-ghz-radar-transceiver:MR3003
[3] V. Giannini, M. Goldenberg, A. Eshraghi, J. Maligeorgos, L. Lim, R. Lobo, D. Welland, C.-K. Chow, A. Dornbusch, T. Dupuis, S. Vaz, F. Rush, P. Bassett, H. Kim, M. Maher, O. Schmid, C. Davis, and M. Hegde, "9.2 a 192-Virtual-Receiver 77/79GHz GMSK code-domain MIMO radar system-on-chip," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 164–166.
[4] S. Kim, A. Rida, V. Lakafosis, S. Nikolaou, and M. M. Tentzeris, "77-GH z mmWave antenna array on liquid crystal polymer for automotive radar and RF front-end module," *ETRI J.*, vol. 41, no. 2, pp. 262–269, Apr. 2019.
[5] O.-Y. Kwon, C. Cui, J.-S. Kim, J.-H. Park, R. Song, and B.-S. Kim, "A compact integration of a 77 GHz FMCW radar system using CMOS transmitter and receiver adopting on-chip monopole feeder," *IEEE Access*, vol. 7, pp. 6746–6757, 2019.
[6] Y.-H. Yang, B.-H. Sun, and J.-L. Guo, "A low-cost, single-layer, dual circularly polarized antenna for millimeter-wave applications," *IEEE Antennas Wireless Propag. Lett.*, vol. 18, no. 4, pp. 651–655, Apr. 2019.
[7] W. Hong, K.-H. Baek, and A. Goudelev, "Multilayer antenna package for IEEE 802.11ad employing ultralow-cost FR4," *IEEE Trans. Antennas Propag.*, vol. 60, no. 12, pp. 5932–5938, Dec. 2012.
[8] M. G. Keller, D. Roscoe, Y. M. M. Antar, and A. Ittipiboon, "Active millimetre-wave aperture-coupled microstrip patch antenna array," *Electron. Lett.*, vol. 31, no. 1, pp. 2–3, Jan. 1995.
[9] C. Cui, S.-K. Kim, R. Song, J.-H. Song, S. Nam, and B.-S. Kim, "A 77-GHz FMCW radar system using on-chip waveguide feeders in 65-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 11, pp. 3736–3746, Nov. 2015.
[10] S.-C. Yen and T.-H. Chu, "An nth-harmonic oscillator using an N-push coupled oscillator array with voltage-clamping circuits," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2003, pp. 2169–2172.
[11] S. Kim, C. Choi, C. Cui, B.-S. Kim, and M. Seo, "A W-band signal generation using N-push frequency multipliers for low phase noise," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 10, pp. 710–712, Oct. 2014.
[12] W. Lee, T. Dinc, and A. Valdes-Garcia, "Reconfigurable 60-GHz radar transmitter SoC with broadband frequency tripler in 45nm SOI CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2019, pp. 43–46.
[13] C.-N. Kuo, H.-S. Chen, and T.-C. Yan, "A K-Band CMOS quadrature frequency tripler using sub-harmonic mixer," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 12, pp. 822–824, Dec. 2009.
[14] W. Ye, K. Ma, K. S. Yeo, and Q. Zou, "A 65 nm CMOS power amplifier with peak PAE above 18.9% from 57 to 66 GHz using synthesized transformer-based matching network," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 10, pp. 2533–2543, Oct. 2015.
[15] Z. Tong, A. Stelzer, and E. Kolmhofer, "77 GHz center-fed differential microstrip antenna array," in *Proc. 5th Eur. Conf. Antennas Propag. (EUCAP)*, Apr. 2011, pp. 583–586.
[16] K. Wincza, S. Gruszczynski, and J. Borgosz, "Microstrip antenna array with series-fed 'through-element' coupled patches," *Electron. Lett.*, vol. 43, no. 9, pp. 487–489, 26 Apr. 2007.
[17] H. Forsten, T. Kiuru, M. Hirvonen, M. Varonen, and M. Kaynak, "Scalable 60 GHz FMCW frequency-division multiplexing MIMO radar," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 7, pp. 2845–2855, Jul. 2020.
[18] R. Feger, C. Pfeffer, and A. Stelzer, "A frequency-division MIMO FMCW radar system based on Delta–Sigma modulated transmitters," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3572–3581, Dec. 2014.
[19] T. Ma, W. Deng, Z. Chen, J. Wu, W. Zheng, S. Wang, N. Qi, Y. Liu, and B. Chi, "A CMOS 76–81-GHz 2-TX 3-RX FMCW radar transceiver based on mixed-mode PLL chirp generator," *IEEE J. Solid-State Circuits*, vol. 55, no. 2, pp. 233–248, Feb. 2020.
[20] *AWR1243 76-GHz to 81-GHz High-Performance Automotive MMIC—TI.Com*. Accessed: Sep. 5, 2020. [Online]. Available: https://www.ti.com/product/AWR1243
[21] M. I. Skolnik, *Introduction to Radar Systems*, 3rd ed. New York, NY, USA: McGraw-Hill, 2001.
[22] H. Van Trees, *Optimum Array Processing*. New York, NY, USA: Wiley-Interscience, 2002.

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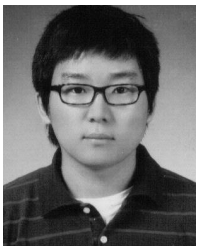

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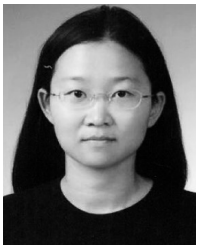

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