A 13 GHz 3:2 Transformer Based Linear Transconductance VCO

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***Abstract*—This paper describes a 13 GHz 3:2 transformer based linear transconductance (LiT) voltage controlled oscillator (VCO) in 65 nm RF CMOS process. Transconductance linearization technique which is simply realized by a 3:2 transformer is used for good phase noise performance. An injection-locked buffer is designed for high output power. The measured output frequency of the proposed VCO shows 12.25 GHz ~ 12.86 GHz and 12.86 GHz ~ 13.52 GHz. The phase noise of the VCO is – 113.94 dBc/Hz at 1 MHz offset frequency. DC power consumption of the VCO core and the buffer is 7.7 mW and 21.6 mW, respectively.**

Keywords-component; CMOS, injection-locked buffer, linear transconductance (LiT) VCO, 3:2 transformer.

I. Introduction

With the recent increase in the demand for low-cost high-integration systems, CMOS has become an attractive solution. Also, many circuit techniques to boost the performance of CMOS process have been reported steadily [1], [2]. In case of CMOS wireless communication systems and radar sensors, achieving a low-phase-noise and high-output-power voltage controlled oscillator (VCO) is one of great concern because the VCO seriously affects the sensitivity of the system. It is generally known that phase noise of CMOS VCOs is fundamentally limited by the oscillation amplitude and the inherent device noise. Thus, linear transconductance (LiT) technique has been reported to solve these problems [2]. In this paper, a 13 GHz VCO with LiT technique which is simply realized by 3:2 transformer is presented.

II. Circuit Description

A schematic of the proposed VCO and the injection-locked buffer is shown in Fig. 1 (a). Different feedback concept for the LiT VCO is required to achieve linearized transconductance, which has lower voltage swing on the drain node than the gate node [2]. The existing LiT VCO is realized by using a capacitive divider for LiT feedback, an LC tank at the gate node, and a choke inductor for V_{DD} biasing. In this paper, however, those components of the existing LiT VCO are simply replaced with one 3:2 transformer [Fig. 1.(b)]. The gate impedance of M1/M2 is higher than the drain impedance of M1/M2 to realize lower voltage swing on the drain node than the gate node because the primary three-turn inductor (324 pH at 13 GHz) and the secondary two-turn inductor (147 pH at 13 GHz) are connected to the gate and the drain of M1/M2, respectively. The output buffer is designed to generate high output power by using the injection-locking (IL) technique which means that the oscillator output frequency is locked into the injected periodic continuous signal frequency [3], [4]. Thus, the IL buffer which oscillates itself at 13 GHz consists of

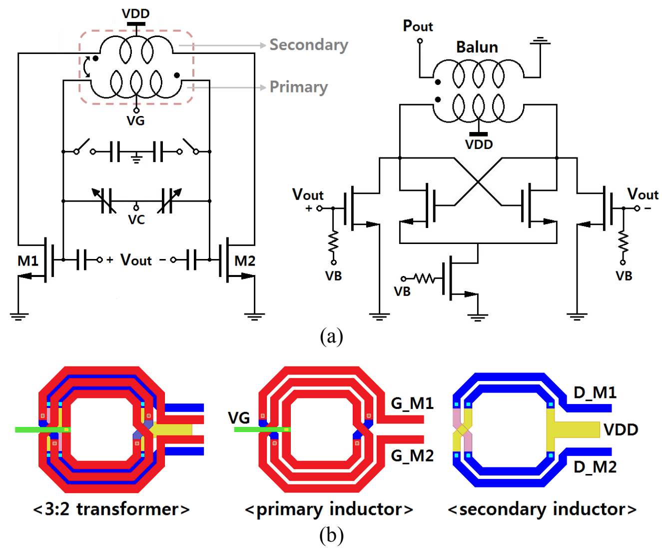

Fig. 1. (a) Schematic of the proposed LiT VCO and the injection-locked buffer (b) Designed 3:2 transformer for LiT VCO

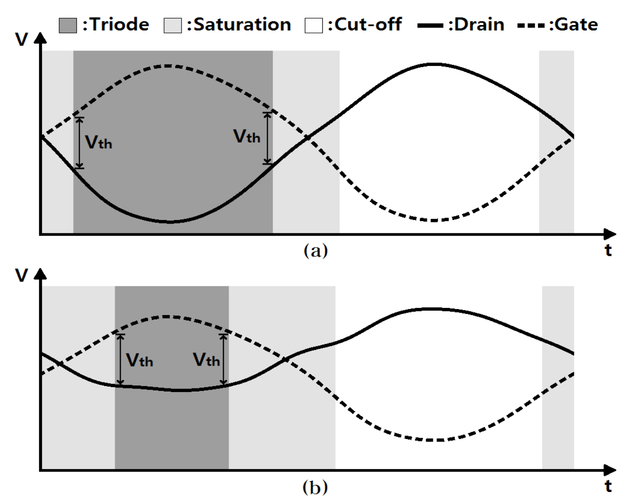

Fig. 2. Simulated gate and drain waveforms of (a) a conventional cross-coupled LC VCO (b) a transformer based LiT VCO

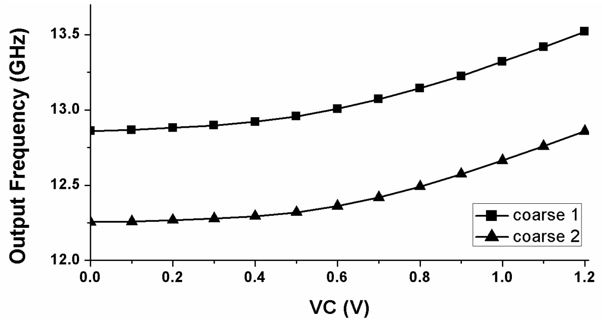

Fig. 3. Measured output frequency

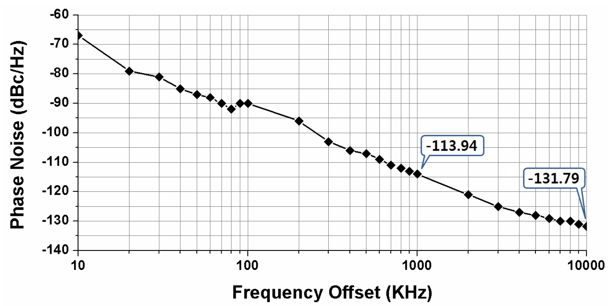

Fig. 4. Measured phase noise when carrier frequency is 13.2 GHz

small-sized transistors which inject the LiT VCO signal to the buffer, a large-sized cross-coupled pair to generate high output power, a current source and a balun.

Simulated gate and drain waveforms of a conventional cross- coupled LC VCO and the proposed 3:2 transformer based LiT VCO are shown in Fig. 2. Due to the impedance difference between the gate and the drain of M1/M2, the drain voltage swing of the 3:2 transformer based LiT VCO is lowered compared to the gate voltage swing. It can diagrammatically found out in Fig. 2 that triode region which is the main source of the transistor nonlinearity is reduced in the proposed VCO. Thus, this VCO can provide good phase noise performance.

III. Measurement Results

The proposed 13 GHz LiT VCO with the 3:2 transformer is fabricated in 65-nm RF CMOS process. The output frequency and phase noise are measured by an Agilent E4448A spectrum analyzer with RF and DC probing. The measured output frequency tuning ranges are 12.25 GHz ~ 12.86 GHz and 12.86 GHz ~ 13.52 GHz [Fig. 3]. The output power is approximately 7.2 dBm when the VCO core and the IL buffer consume 7.7 mW and 21.6 mW, respectively. The measured phase noise shows a good value of -113.94 dBc/Hz at 1 MHz offset frequency [Fig. 4]. Fig. 5 shows a micro-photograph of a chip. The chip size is 830 × 530 μm^2, including test pads. Table I highlights the details of the VCO performance. The FOM is determined as below.

$$FOM = -L(\Delta f) - 10\log\{(\Delta f / f_{osc})^2 \cdot P_{dc\_mW}\} \qquad (1)$$

$L(\Delta f)$ is the phase noise, Δf is the offset frequency, f_{osc} is the oscillation frequency and P_{dc_mW} is the DC power consumption.

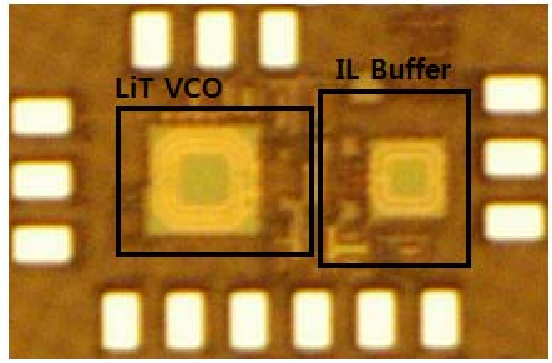

Fig. 5. Chip micro-photograph

TABLE I. Performance of the Proposed VCO

Technology	65 nm RF CMOS
Tuning Range	Coarse 1: 12.25 ~ 12.86 GHz Coarse 2: 12.86 ~ 13.52 GHz
Phase Noise	-113.94 dBc/Hz @ 1MHz offset
Core DC power	7.7 mW
Buffer DC power	21.6 mW
Output power	7.2 dBm
Full-Chip Size	830 × 530 μm^2
FOM	187.48

IV. Conclusion

A 13 GHz 3:2 transformer based linear transconductance VCO is presented in the paper. The proposed LiT VCO achieves good phase noise performance without additional components compared to an existing LiT VCO becuase the transformer with different turn ratio between the primary (three-turn) and the secondary (two-turn) inductor performs not only an LC tank but also LiT operation.

Acknowledgment

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Ministry of Science, ICT & Future Planning (MSIP) (No. 2009-0083495). This work was supported by the IDEC.

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