A Dual Band CMOS Power Amplifier for an S/X Band High Resolution Radar System

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***Abstract* — This paper presents a dual band CMOS power amplifier (PA) for an S/X band high resolution radar system. Reconfigurable band-switchable matching networks and a dual band Wilkinson power combiner (impedance transformer) are used for an output matching network. The PA is fabricated using a UMC 0.13 μm CMOS process. It provides a saturated output power of 24.8 dBm and 25.3 dBm with the power-added-efficiency (PAE) of 27.2 % and 36.4 % at 8.4 GHz and 3.0 GHz, respectively. The 3-dB bandwidth is 2.5 GHz (7.4-9.9 GHz) and 2.3 GHz (2.7-5.0 GHz). This amplifier achieves a fractional bandwidth of 29% and 60 % at each band, and shows suitable performance for use in a high resolution radar system.**

***Index Terms* — Dual band, CMOS, power amplifier (PA), switch, radar system.**

I. Introduction

In radar system, the appropriate frequency band differs according to the environment (e.g., obstacles, weather, targets, etc.). For example, frequency bands higher than the X-band suffer severe weather and atmospheric attenuation, which limits radar systems utilizing these frequency bands to short range applications[1]. Therefore, it is desired to develop design approaches for dual band radar system which can use appropriate frequency band in different situations. The bandwidth of each band is also very important because the range resolution of a radar system is determined from its bandwidth. Achieving a dual band function with a wide bandwidth at each band is particularly difficult for power amplifiers (PAs), due to the inherent narrow band characteristics of the matching networks. Most of the reported dual band PAs are not appropriate for radar systems because they are not large enough for the frequency difference between two bands and/or the bandwidth of each band is too narrow for use in a high resolution radar system.

Several approaches have been developed to implement dual band PAs. One approach is to employ electronically tunable devices such as varactors, variable inductors, and PN diodes to adjust the inductance or capacitance[2]. This approach is only appropriate when the frequency difference between each band is narrow; otherwise, degradation in reliability and performance occurs. Another approach is to use a parallel/series resonant LC structure to a matching network, but this is only applicable to narrow band PAs[3].

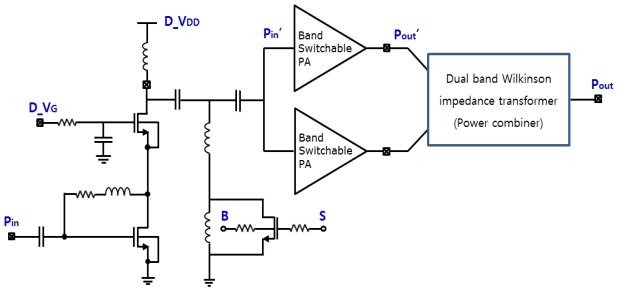


Fig. 1. A 2-stage dual band CMOS power amplifier

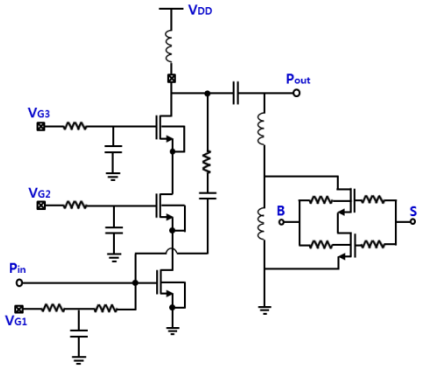


Fig. 2. A 3-stacked band switchable power cell of Fig. 1

In this paper, we propose an S/X dual band PA design technique for a high resolution radar system by exploiting a reconfigurable band-switchable matching network. Detection of small targets (7 cm) requires that, the 3-dB bandwidth of each band cover a wider bandwidth than 2.15 GHz. A stacked structure, switches and a Wilkinson power combiner are adopted to meet these requirements. A wide bandwidth is obtained by using a structure that combines two stacked PAs to achieve a high R_{opt} (optimum PA load impedance). The output matching network is designed into a 2-stage through the switched inductor (on-chip) and the dual band Wilkinson power combiner (off-chip), which can perform impedance transforming for low-Q matching[4],[5]. The switch allows the required

value of shunt inductance for impedance matching to be used in each band. Therefore, even though a large frequency difference exists between the dual bands, an efficient impedance matching is possible. The 3-dB bandwidth is 2.3 GHz / 2.5 GHz at the S/X band so it can detect a target with 6.5 cm / 6.0 cm range resolution.

II. Design of Dual-Band CMOS PA

The PA designed in this paper operates as an S/X dual band. When it operates as an X-band, the switch is turned on and the switched inductor looks like a short. If it operates as an S-band, the switch is turned off. Fig. 1 shows the circuit of the 2-stage dual band PA. The main stage PA is designed as a 3-stacked structure. A triple-well CMOS process is used for this PA and the p-well of each transistor is tied to avoid body effect and drain-bulk breakdown. The input power enters into two identical 3-stacked power cells and the switched inductor and two capacitors are employed to match the Z_{opt} (18+jX) of the S/X bands to 35 Ohm. Fig. 2 shows the single power cell that has been matched to 35 Ohm. The dual band Wilkinson power combiner allow, both the power combining and the impedance transformation from 35 Ohm to 50 Ohm.

The driver stage is designed as a feedback amplifier to prevent bandwidth reduction because of the input matching. The required input power of the main stage of the X-band is about 5 dB higher than for the S-band. Use of the feedback amplifier restrains the low frequency gain and rewards the high frequency gain, so the input power of the 2-stage PA can be similarly matched at each band. An additional benefit is gained from a size perspective because broadband impedance matching is possible with a small number of components.

III. Matching Network Design with Switch

A few issues arise when CMOS process is used as switch. First, a CMOS switch should be realized by a triple well transistor in order to control body voltage, so a problem of body junction diode turn-on can occur. When a large ac signal comes into the source_(drain), the P-well of the body has periods of a more positive voltage than the N+ region of source_(drain). As a result, the diode is turned on. Second, if a voltage lower than that of the gate node is applied to the source_(drain), the switch will be turned on unintentionally when it should be off. The last problem is breakdown of the transistor. The switches that are employed in this paper are designed with these problems.

A. CMOS switch for PA's matching network

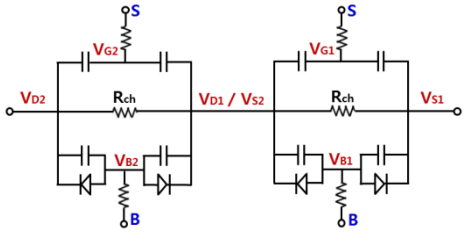


Fig. 3. A 2-stacked switch equivalent circuit of Fig 2.

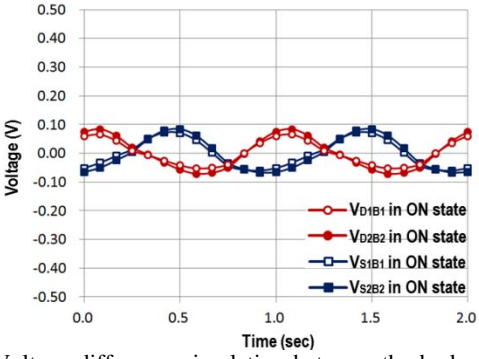


Fig. 4. Voltage difference simulation between the body and the source_(drain) in Fig. 3 (ON state)

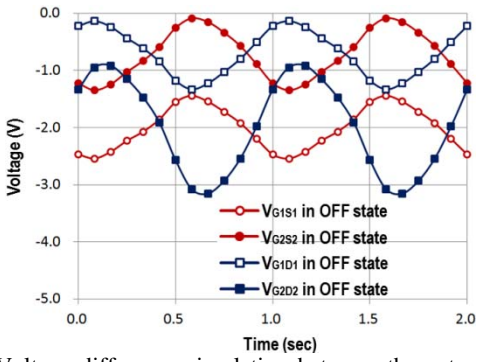


Fig. 5. Voltage difference simulation between the gate and the source_(drain) in Fig. 3 (OFF state)

The switches are used for the output and interstage matching networks. A breakdown is prevented by designing the switch in 2-stacked structure so that it can be acted as a voltage divider through parasitic capacitance[6]. Fig. 3 shows the 2-stacked switch equivalent circuit. In addition, large resistors are connected to the body to prevent the problem of junction diode turn-on when the switch is in the on-state. Therefore, the body voltage follows the signal voltage swing, which comes into the source_(drain). Fig. 4 shows that the voltage difference between the body and the source_(drain) is lower than the diode turn-on voltage. Lastly, a negative voltage is applied to the gate and the body to prevent generation of a channel in the transistor when the switches should be turned off. Fig. 5 shows that the voltage

difference between the gate and the source_(drain) is lower than the threshold voltage of the transistor.

B. Output and interstage matching networks

The output matching network is 2-stage to obtain a wide bandwidth in each band. Because of stacked structure, R_{opt} in the S/X bands of the PA is about 18 Ohm, which is much higher than that of parallel FET structure. An NMOS switch is used to control the value of the shunt inductance to match the Z_{opt} (18+jX) of the S/X bands to 35 Ohm. The impedance matching from 35 Ohm to 50 Ohm can be done using the dual band Wilkinson power combiner.

The interstage matching network is designed with two series capacitors, a shunt inductor, and a switch. A single switch is used because the voltage swing is not as large as that in the output matching network. The driver stage is designed so that the values of the device and components are optimized to consider the interstage matching. In addition, on the Smith chart, the outside points are matched from the inside points for a wide bandwidth.

IV. Measurement Results

A photograph of the S/X dual band CMOS PA is shown in Fig. 6. It is fabricated with a 0.13 μm 1P8M CMOS technology. The chip area is 1.116 mm x 0.765 mm including the pads. A printed circuit board for testing the PA was also fabricated using Rogers Duroid 5880 substrate.

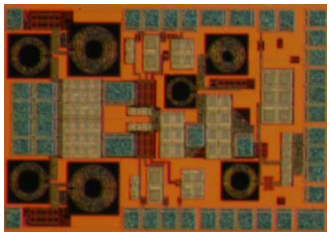
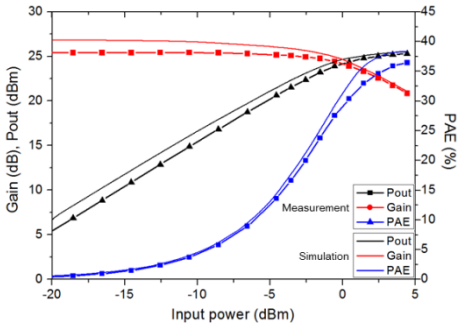


Fig. 6. Chip photograph of the PA

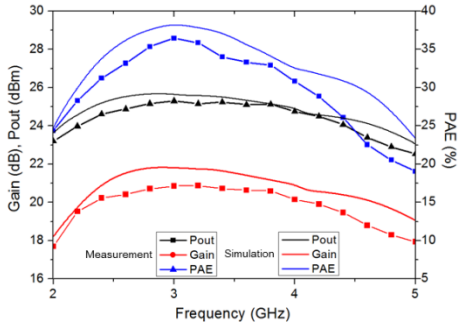
The drain bias voltages are 1.8 V for the driver stage and 3.6 V for the power stage. The gate bias voltages are 1.2 V for the driver stage and 0.7, 1.9, and 3.1 V for the power stage. The amplifier consumes DC current of 296 mA; that is, 240 mA for the power stage, and 56 mA for the driver stage.

A. S-band measurement results

The PA achieves a peak small signal gain of 25.9 dB at 3.0 GHz with its 3-dB bandwidth in the frequency range of 2.7-5.0 GHz. Fig. 7(a) shows the measured power transfer characteristic at 3.0 GHz. The PA has a P_{sat} of 25.3 dBm and a PAE of 36.4 %.



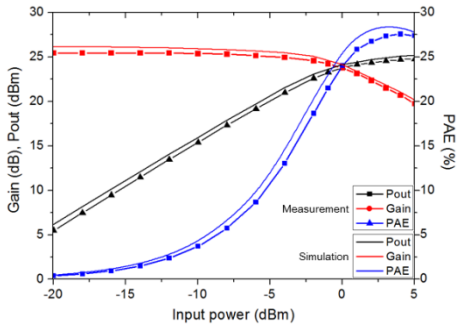
(a)



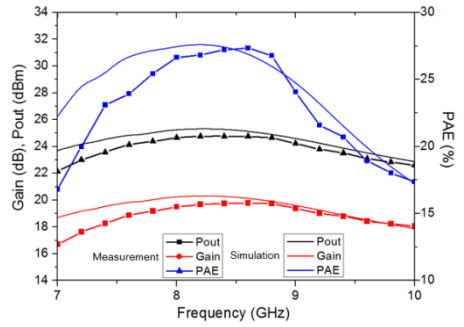
(b)

Fig. 7. Simulated and measured power characteristics of the 2-stage PA at S-band (a) Input power sweep at 3.0 GHz. (b) Frequency sweep at P_{IN} = 5 dBm.

B. X-band measurement results



(a)



(b)

Fig. 8. Simulated and measured power characteristics of the 2-stage PA at X-band (a) Input power sweep at 8.4 GHz. (b) Frequency sweep at P_{IN} = 5 dBm.

TABLE I
SUMMARY OF X-BAND PAS

Ref.	Process	Technique	VDD (V)	Frequency (GHz)	Gain (dB)	P_{out} (dBm)	PAE (%)
[7]	0.18 µm CMOS	push-pull with transformer	3.3	8.5 – 10.0 (@ 8.5 GHz)	29.0	23.5	19.0
[8]	0.18 µm CMOS	Push-pull with transformer	3.0	8.6 – 10.3 (@ 10.0 GHz)	25.0	24.5 (P_{1dB} = 22.0)	18.0
[9]	90 µm CMOS	push-pull with transfor. and ind.	N/A	5.2 – 13.0 (@ 8 GHz)	17.5	25.2 (P_{1dB} = 22.6)	21.6 (15.2 @ P_{1dB})
[10]	0.18 µm CMOS	push-pull with transformer	3.6	6.5 – 13.0 (@ 9.5 GHz)	25.3	21.5 (P_{1dB} = 20.2)	20.3 (14.8 @ P_{1dB})
This work	**0.13 µm CMOS**	**stack / switchable matching network**	**3.6**	**7.4 – 9.9 (@ 8.4 GHz)**	**25.9**	**24.8 (P_{1dB} = 22.9)**	**27.2 (17.3 @ P_{1dB})**
				2.7 – 5.0 (@ 3.0 GHz)	**25.4**	**25.3 (P_{1dB} = 23.1)**	**36.4 (23.5 @ P_{1dB})**

The PA achieves a peak small signal gain of 25.4 dB at 8.4 GHz with its 3-dB bandwidth in the frequency range of 7.4-9.9 GHz. Fig. 8(a) shows the measured power transfer characteristic at 8.4 GHz. The PA has a P_{sat} of 24.8 dBm and a PAE of 27.2 %.

Tablel summarizes the characteristics of the proposed PA and other CMOS PAs. In comparison with the other listed PAs, this amplifier achieves high output power and the highest PAE at the X-band even though it achieves dual band function.

V. CONCLUSION

In this paper, a CMOS S/X dual band PA was developed using 0.13 µm 1P8M CMOS technology. The CMOS switch, which is a key element of the PAs, has been designed with transistor breakdown, junction diode turn-on, and an unintentional turn-on of the switch. The dual band PA consists of two stages with interstage and output matching networks. It provides a saturated output power of 24.8 dBm and 25.3 dBm with a PAE of 27.2 % and 36.4 % at 8.4 GHz and 3.0 GHz, respectively. The 3-dB bandwidth is 2.5 GHz (7.4-9.9 GHz) and 2.3 GHz (2.7-5.0 GHz). This amplifier achieved fractional bandwidths of 29 % at the X-band and 60 % at the S-band, and achieved suitable performance for use in a dual band high resolution radar system.

ACKNOWLEDGEMENT

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