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BRIEF PAPER

7-Bit Multilayer True-Time Delay up to 1016 ps for Wideband Phased Array Antenna

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SUMMARY We present a seven-bit multilayer true-time delay (TTD) circuit operating from 1 to 7 GHz for wideband phased array antennas. By stacking advanced substrates with low dielectric loss, the TTD with PCB process is miniaturized and has low insertion loss. The signal vias with surrounding ground vias are designed to provide impedance matching throughout the band, allowing the overall group delay to be flat. The standard deviation of the TTD for all states is below 19 ps, which is 1.87% of the maximum group delay. The maximum delay is 1016 ps with resolution of 8 ps. The implemented TTD is 36.6×19.4 mm^2 and consumes 0.65 mW at 3.3 V supply for all the delay states. The measured input/output return loss is better than 12.1 dB for the band of 1–7 GHz.

key words: *true-time delay, wideband phased array, multilayer PCB, signal via*

1. Introduction

Phased array antennas are widely used in wireless communications and radar systems [1], and the design of these systems usually requires ever-increasing bandwidth [2]. However, a phased array antenna with phase shifter can only operate in a narrow band, resulting in a beam squint phenomenon [3], [4]. Unlike a phased array antenna using phase shifters, a phased array antenna with TTDs solves this problem and enables beamforming in a wide band [5]. Therefore, TTD is required in wideband phased array antenna systems.

TTDs must present several features such as low insertion loss, long total delay, low phase distortion, and compact size. In beamforming systems with relatively low frequency band, such as the S- and C-bands, a long delay time allows beam steering, because the distance between antenna elements is long. In addition, as the number of antenna elements increases, the delay time should be longer. Still, designing a TTD with long delay using an IC results in a large insertion loss [6], and the IC process is expensive. Alternatively, a PCB process is less expensive, but the resulting TTD can be larger.

Aiming to TTD miniaturization using a PCB process, in this study we designed a multilayer TTD with long delay time by stacking advanced substrates with low dielectric loss.

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2. Design of TTD

2.1 Design Considerations

Generally, phase shifters are used for narrowband operation of phased array antennas, as using them for wideband distorts the beam steering angle by a phase depending on frequency, conforming the beam squint phenomenon. TTD lines are used to prevent this phenomenon. Figure 1 shows a linear array antenna with distance d between antennas. The time delay between each antenna in free space can be expressed as

$$\Delta t = \frac{d \sin\theta}{c}, \tag{1}$$

where c is the speed of light and θ is the scanning angle.

A recently published TTD circuit, a trombone-like structures [6], combining gm-RC and LC delay network, achieves flat delay [7], [8]. However, compared with passive TTD circuits, these active solutions consume a certain power meanwhile exhibiting a limited linearity performance. Switch-based solutions such as a switched-TL and a switched LC-network provide an alternative way to achieve low insertion loss and a large delay tuning range while keeping Z0 constant when configuring TTD [9], [10]. Figure 2

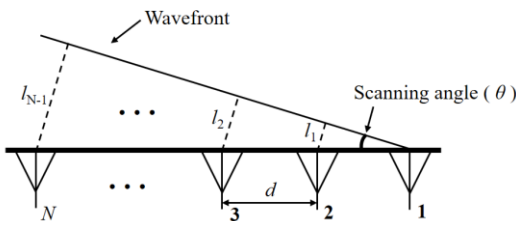

Fig. 1 Linear array with N elements.

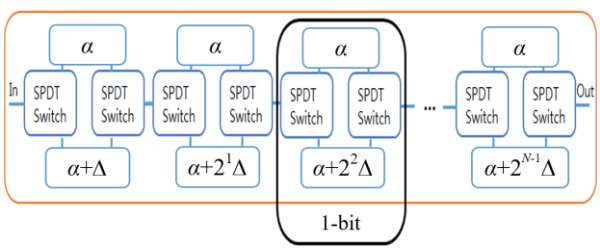

Fig. 2 Block diagram of TTD line.

illustrates a switched line structure typically used in TTD lines. Two single pole double throw (SPDT) switches are needed for a one-bit line. In the figure, α is a reference line and Δ is a line with a delay time longer than the reference line by a minimum amount (i.e., resolution time). By arranging doubling Δ in series, it is possible to efficiently construct a TTD line with minimum delay time resolution.

Several considerations are necessary in the design of a switched line TTD. First, resonance of line coupled by the off-state capacitor of the SPDT should be avoided [11]. Resonance can cause delay distortion when the electrical length of a line connected through this capacitor is an integer multiple of a half wavelength. To prevent this distortion, a switch with an off-state isolation of at least 30 dB should be used. We prevented resonance by using the HMC1118 switch (Analog Devices, Inc., Norwood, MA, USA) that provides excellent isolation in the desired frequency band [12]. In addition, the reflected wave generated by discontinuity and impedance mismatch can affect the phase between input and output, which can in turn deteriorate the TTD performance [13]. Hence, multilayer fabrication should consider the signal passing through a via and matching should be carefully performed.

2.2 TTD Resolution and Number of Bits

When designing a TTD line for wideband beam steering of an N-element array antenna, the required maximum delay and number of bits are determined by the desired beam steering angle and resolution [8]. We designed a TTD for an eight-element linear array operating at maximal beam steering angle of 60° and resolution of 5°. The frequency band was set to 1–7 GHz according to the operating band of the switches. The frequency range of the TTD includes the operating frequency range of UWB radars [14], [15]. As shown in Fig. 1, the minimum value of the electrical length in air is $l_1 = d \times \sin(5°)$ and the maximum value is $l_7 = 7d \times \sin(60°)$. Generally, when designing a broadband antenna, the distance between antennas at the lowest frequency should have a relatively small wavelength to avoid the generation of a grating lobe at the highest frequency [16]. Therefore, we set the distance between antennas to 37.5 mm, which is 0.125 of the wavelength of 1 GHz. In this case, the delay time has a minimum of 10.9 ps and a maximum of 757.8 ps. The number of bits of the TTD is at least seven, as determined by $l_7 \leq l_1 \times 2^n$. Hence, we designed a seven-bit TTD with minimum and maximum delay time of 8 and 1016 ps, respectively. A unit cell was designed to implement desired delay by repeating it. We performed electromagnetic simulation, including measurement results of the switch, using CST Design Studio (Computer Simulation Technology GmbH, Darmstadt, Germany).

For miniaturization, we implemented a multilayer structure. In the first layer, the switch was placed on the substrate by soldering, and microstrip lines were arranged to form short lines. The two longest lines, corresponding to the two most significant bits, were implemented using

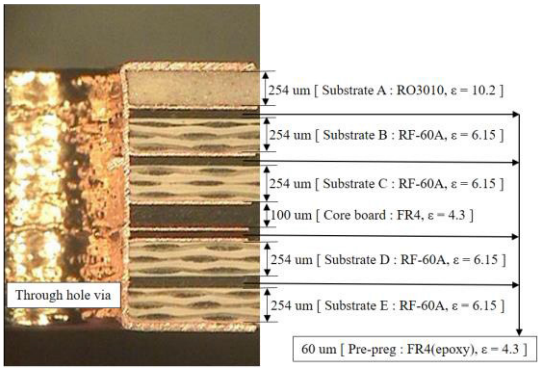

Fig. 3 Cross-sectional view of multilayer PCB and layer characteristics.

stripline in the second and third layers to reduce the total form factor of the TTD. Comparing multilayer PCB with conventional single layer PCB, if a delay line with a delay time of 256 ps and 512 ps is implemented by a microstrip, an area of 78.6 mm^2 and 157.2 mm^2 respectively is required even if the high-permittivity substrate is used. Considering the change of the entire size, it can be seen that an additional 34% area is required if a single layer PCB is used to implement the TTD of the same performance. The arrangement of the switches can not be freely set in TTD using single layer PCB, therefore the practical required area is twice or more. This can be confirmed in Table 1 [18]. The cross-section of the fabricated TTD layers is shown in Fig. 3, detailing the layer characteristics. The RF-60A is a low-loss substrate provided by Taconic, which is twice as cheap as Rogers substrate, and is suitable for low-cost compact and low-loss TTD.

2.3 Optimal Design of Signal via

The most important part of stacking advanced substrates is the design of signal via. As a via introduces discontinuity in the transmission line, a matching structure is required to mitigate the reflected wave. In fact, multiple reflected waves can be added at the output, resulting in phase distortion of the TTD. As shown in Fig. 4, we designed three types of signal vias. Specifically, ViaA is intended for transition from the top microstrip line to the microstrip line of the motherboard. ViaB is intended for transition from the top microstrip line to the stripline of the second layer, and ViaC for transition from the top microstrip line to the stripline of the third layer.

The signal via circuit model is shown in Fig. 5 [17]. Series L is the inductance of the via body and shunt C is added to the various capacitance values, as shown in Fig. 6. The impedance of the signal vias should match the wideband load impedance to ensure good signal transition. The two most significant bits were composed of striplines in the second and third layers to reduce the total area using ViaB and ViaC, respectively. By adjusting the inductance and capacitor values by changing the radii of anti-pad ($R1$), via ($R2$), pad ($R3$), and distance between vias enables impedance

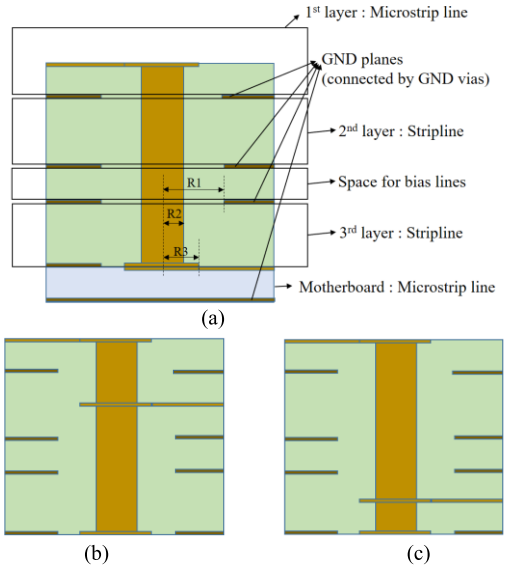

Fig. 4 Side-view of vias: (a) ViaA, (b) ViaB, and (c) ViaC.

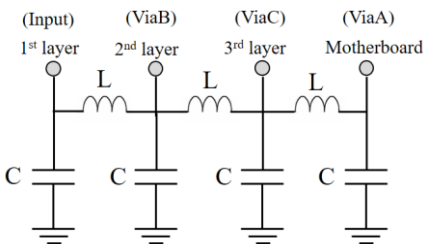

Fig. 5 Equivalent circuit of a via.

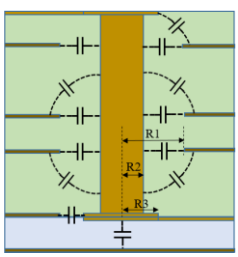

Fig. 6 Capacitance of each via.

matching. The most dominant factor is the radius of anti-pad ($R1$), which is the distance between the ground plane and the signal via, i.e., the diameter of the hole in the ground conductor plate to allow the via to pass through ground.

Figure 7 shows the measured matching characteristics of signal vias while changing the radius of the anti-pad. The optimal result can be obtained by adjusting this radius, as confirmed from the measurements. The black solid line in Fig. 7 shows the radii of anti-pad with the best matching conditions in the bandwidth of 1–7 GHz, being 0.85 mm for ViaA, 1.2 mm for ViaB, and 1 mm for ViaC. Notice that the optimal radii of anti-pad depends on the type of via.

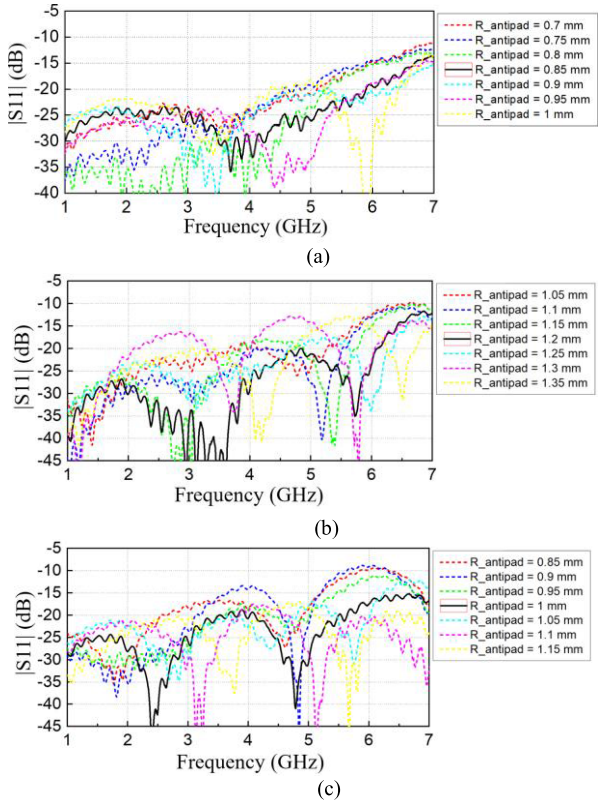

Fig. 7 Measurements of signal via according to radius of anti-pad: (a) ViaA, (b) ViaB, and (c) ViaC.

3. Experimental Results and Discussion

We fabricated the proposed seven-bit multilayer TTD in a PCB process, and its photo is shown in Fig. 8. The resulting TTD has an area of $36.6 \times 19.4\,\text{mm}^2$. The power consumption of the SPDT switches for all delay states is 0.65 mW at 3.3 V supply.

The measured input and output reflection coefficients of the major delay states are shown in Fig. 9 (a). The measured input/output return loss is better than 12.1 dB across the bandwidth of 1–7 GHz. The insertion losses of the TTD are shown in Fig. 9 (b). The losses of the 14 switches used in the TTD are 7 dB at 1 GHz and 9 dB at 7 GHz, and additional loss occurs over the lines and vias.

The measured phase delay with reference to the shortest delay of the TTD is shown in Fig. 10, with standard deviation of the TTD for all the states below 1.4 ps. The measured group delay of the TTD is shown in Fig. 11, with standard deviation of the TTD for all the states below 19 ps, which is 1.87% of the maximum group delay.

The measured performance is summarized and compared with that of other TTD circuits in Table 1. Our approach shows an improved performance regarding a figure of merit defined as the relative delay divided by the insertion loss at the longest delay state, a large number of bits of resolution, and low power consumption. A high FoM means

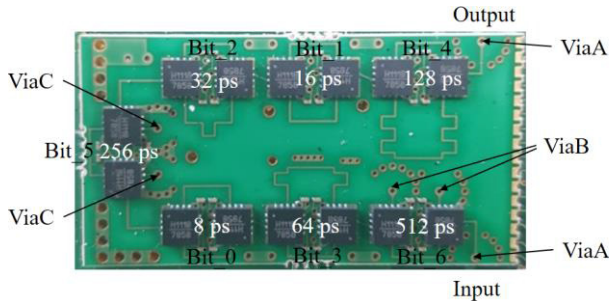

Fig. 8 Fabricated TTD in PCB process.

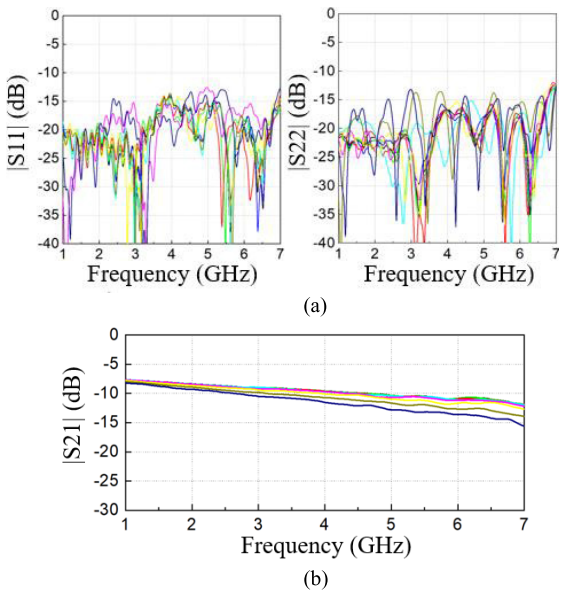

Fig. 9 Measured (a) input/output reflection coefficients and (b) insertion loss of the TTD for the main bits.

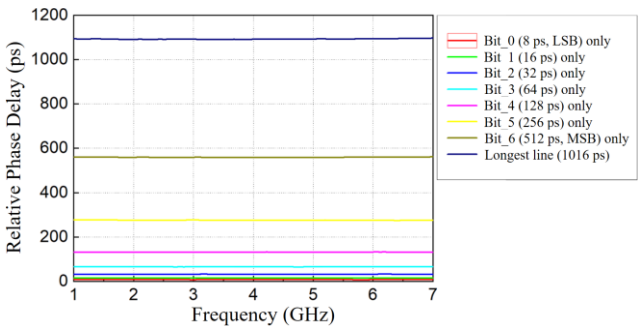

Fig. 10 Measured phase delay with respect to the shortest delay state of the TTD.

that less loss is required in implementing TTD with the same delay than other papers. In case that a large delay time is required such as phased array in C-band or S-band, MMIC TTDs have a huge loss compared with the proposed TTD. In addition to low loss, the proposed TTD has an advantage in terms of cost. Even though the price of SPDT switches is included with the cost of PCB process, it is much cheaper than the price of MMIC. Therefore, the proposed TTD with

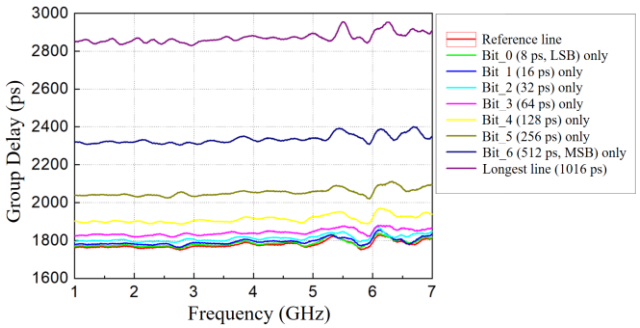

Fig. 11 Measured group delay of the TTD.

Table 1 Comparison with previously reported design.

	[6]	[7]	[8]	[9]	[18]	This work
Substrate	CMOS	CMOS	PHEMT	GaAs	PCB	PCB
Frequency (GHz)	1–20	1–21	2–20	0–40	8–12	1–7
Maximum delay (ps)	400	274	145	87	97.3	1016
Insertion loss @ 7 GHz (dB)	24.5	11.2	11	2.5	3.7	15.6
*FoM @ 7 GHz (ps / dB)	16.3	24.5	13.2	34.8	26.3	65.1
Number of bits	6	3	6	4	5	7
Size (mm^2)	4	1.1	5.6	30	**3710	710
DC power (mW)	2.6–6	2–6.2	30	n/a	n/a	0.65

*FoM = maximum delay / Insertion loss, figure of merit

**Since the full size is not presented in [18], the estimated value from the given values of line length is used in table.

low loss characteristic, low cost, low power consumption and a large maximum delay time can be a good solution for many wireless applications.

4. Conclusion

We propose a 1–7 GHz seven-bit multilayer TTD with group delay range of 1016 ps at 8 ps steps using a PCB process. We achieved miniaturization of the PCB-based TTD by stacking advanced substrates. As the low-loss substrate is laminated, the TTD has low insertion loss. The signal vias, which are essential for multilayer fabrication, suitably matched with the careful selection of anti-pad radius according to the via type, resulting in a flat delay over the band. The standard deviation of the TTD for all states is below 19 ps, which is 1.87% of the maximum group delay. The proposed TTD can be used effectively as a low-cost signal processing block for 1–7 GHz wideband phased array systems.

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