Propagation Velocity Equalizer Circuit on Multi Microstrip Transmission Line Structure

Jaejun Lee*, Byungjoon Kim and Sangwook Nam

School of Electrical Engineering and Computer Science,

INMC, Seoul National University, Seoul, Korea

* *Jaejun Lee is also with Samsung Electronics Co. Ltd. Hwasung 445-701, Korea*

jaejun@ael.snu.ac.kr

***Abstract*— This paper proposes an equalizing method to enhance the timing margin of high-speed digital signals for multi-conductor transmission lines in inhomogeneous media. This equalizer is activated when the system sets up the initial state such as the booting state of personal computers and determines the values of capacitors between the adjacent lines. Therefore, the equalizing circuit does not consume the additional current during the operation of the system. For the 100mm five-line coupled M-MTL, the simulated total peak-to-peak jitter including crosstalk noise was 89 ps before equalizing whereas the M-MTL with the proper values of additional capacitance between the adjacent lines by the equalizer, showed 46 ps jitter.**

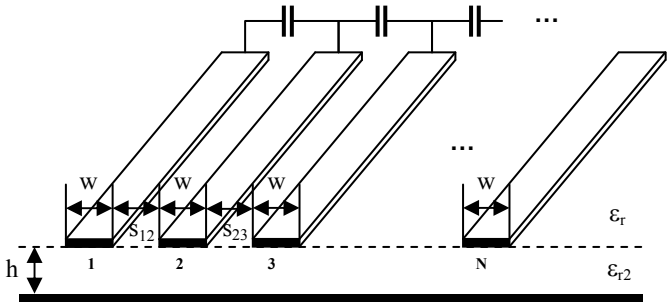

Fig. 1 Concept of propagation velocity equalization

I. INTRODUCTION

Current high-speed portable systems allow only a small routing area for chip-to-chip interconnection, requiring increased density of interconnections. Additionally, the spacing between the transmission conductors has been reduced. Consequently, crosstalk due to the coupling between transmission lines is expected to be the primary limiting factor in printed circuit board (PCB) design. In chip-to-chip communication, the microstrip multi-conductor transmission line (M-MTL) is one of the popular routing structures but this structure can easily produce serious far-end crosstalk due to its inhomogeneity.

Many papers have researched equalizer circuits used to eliminate distortion, such as crosstalk-induced-jitter (CIJ) at the receiver block including the feed forward equalizer and the decision feedback equalizer [1]–[3]. These equalizer schemes may be good solutions to the crosstalk noise problem; however, they are not suitable for low-power and low-cost systems. Moreover, many papers have discussed the reduction of CIJ using passive elements. These papers have proposed to resolve CIJ by inserting capacitors between lines to equalize the velocities of the even/odd modes that exist in the two lines involved [4]–[6]. However, these methods are not adaptive solutions. Therefore, when PCB routing structures are changed, the values of the inserted capacitors must be changed to reduce CIJ.

In this paper, we suggest a circuit scheme to obtain more accurate values for the compensation capacitors that match the mode velocities in M-MTL, so that the timing margin is enhanced and the eye-diagram deterioration is minimized. This method can be applied to high-speed signaling through a parallel link.

II. THE PROPOSED METHOD

In this study, we consider interconnections with N transmission conductors and a reference conductor in an inhomogeneous medium ($\varepsilon_{r1} \neq \varepsilon_{r2}$) that provides N transmission channels as shown in Fig. 1. Hence, there are N different orthogonal modes that can propagate with different propagation constants, creating CIJ in this structure. In other words, the far-end crosstalk phenomenon induces both the transient far-end crosstalk voltage (V_{FE}) waveform and the crosstalk-induced timing jitter (CIJ) at the receiver side. [3]

$$V_{FE}(t) = \frac{1}{2} \cdot \sqrt{L_S \cdot C_T} \cdot \left(\frac{C_M}{C_T} - \frac{L_M}{L_S} \right) \cdot \frac{dV_a(t - TD)}{dt} \qquad (1)$$

$$\Delta TD = \sqrt{L_S \cdot C_T} \cdot \left(\frac{L_M}{L_S} - \frac{C_M}{C_T} \right) \qquad (2)$$

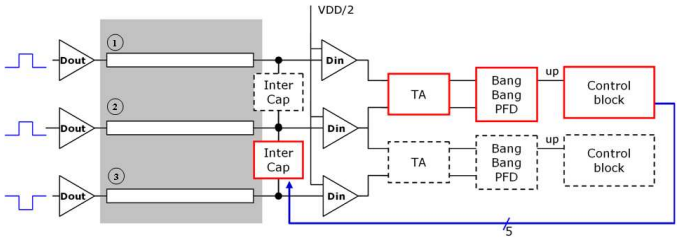

Fig. 2. Block diagram

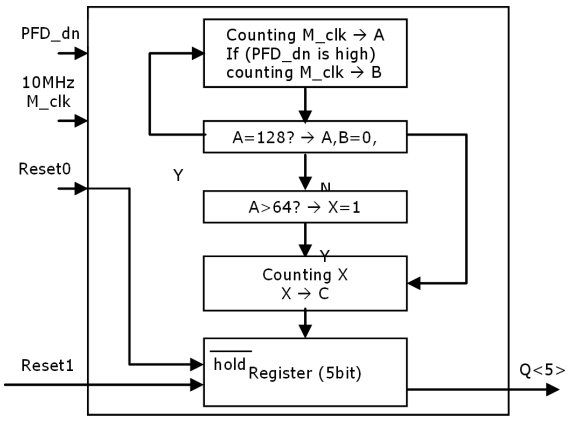

Fig. 3 Algorithm of the decision on interline capacitor values

From (1) and (2), we can see that both can be reduced by decreasing the difference between the inductive and capacitive coupling ratios. Furthermore, this difference was reduced by increasing the mutual capacitance C_M as shown in Fig. 1.

The proposed propagation velocity equalizer circuit is for determining of the additional mutual capacitance value. This equalizing circuit operates when the system sets up the initial state, such as a booting state of the personal computer. When the values of interline compensation capacitor (intercap) in the capacitor block are fixed, we do not have to operate this equalizer again. Therefore, the equalizing circuit does not consume additional current while the real system is operating.

To find the different propagation time on M-MTL, a special combination of output drivers must be stimulated. In the case of a three-coupled M-MTL structure, output drivers of line 1 and line 2 stimulate high going edges, whereas the driver of line 3 must be a low going edge as shown in Fig.2. In this situation, the wave at the end of line 2 is faster than the wave in line 1 since line 2 is affected by line 3. Therefore, this difference between the line 1 and line 2 can determine the capacitor value between line 2 and line 3. Under this condition, the equalizer circuit is operated. To determine the capacitance values in an intercap circuit block, input data receiver (Din), time amplifier (TA) and a bang-bang phase frequency detector (PFD) are used as shown in Fig.2.

The intercap block consisted of the MIM capacitor array with 31 different values from 0pF to 2pF. TA increases the time difference between two transmission lines 5 to 6 times. After Improved time difference resolution by TA, the PFD

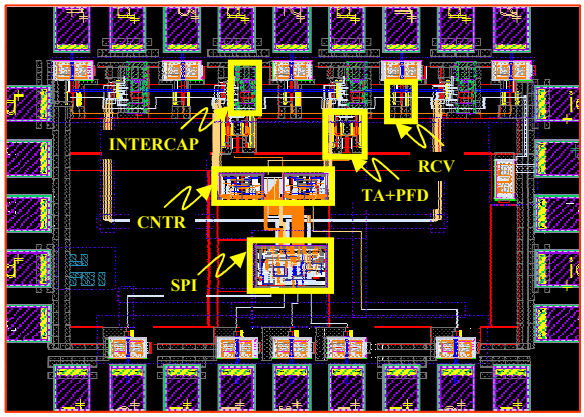

Fig. 4 Layout of the propagation equalizer circuit.

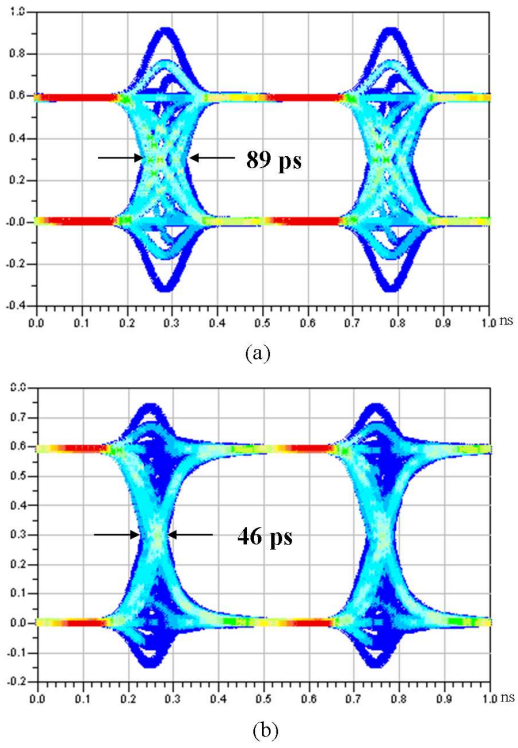

Fig. 5 (a) simulated eye diagram without the proposed equalizer (b) simulated eye diagram with proposed equalizer on the condition of CIJ at the center line of the five-line coupled MTL.

determines which one is faster. The signal from the PFD is used in the control block which determines the intercap value.

If unwanted noise is invoked in the equalizing, the control block can give misleading intercap values. Therefore, the proposed control block (CNTR) accepts the procedure that has been determined the faster one using the majority voting algorithm as shown in Fig.3. It means that the control block count on the PFD output till 128 and catches the PDF output only when that value is above 64. And, the control block needs several command pins. To reduce the number of the die pad, a serial to parallel interface (SPI) is applied to the chip.

The proposed equalizer was designed and laid out using UMC 0.13μm CMOS technology with 0.8mm×1.0mm die size as shown in Fig. 4.

III. Results

To validate the proposed method, the post layout simulation was performed for M-MTL with five 100mm-length coupled 50Ω lines on an RO4350B substrate with a ε_r, thickness and width of 3.48, 0.762mm, and 1.480mm, respectively. Fig. 5 shows the jitter difference between before equalization and after equalization in the case of 0.5mm coupled line space with the pseudo-random-bit-sequence (PRBS) signals utilizing 1.2V V_{DD} injected. By the result of this simulation, the jitter has an improvement of 48.3% after the proposed equalization has been performed. Therefore, this proposed method is helpful in reducing the crosstalk even though this equalization does not offer fully reject the crosstalk noise.

IV. Conclusions

In this paper, an effective implementation was proposed for partial passive equalization of the propagation velocities of modes in M-MTL. According to the simulation, the jitter was reduced by 48.3% after the proposed equalization was used. The proposed technique is suitable for relatively short and dense channels that have no guard trace like memory systems since this crosstalk equalization technique offers low-cost, low-power implementation.

Acknowledgment

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