A Wideband stacked Linear Power Amplifier in 0.11μm CMOS

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I. INTRODUCTION

As the number of standards being supported per end-user cellular devices increases, implementing high performance multiband multi-mode (MBMM) linear power amplifiers is highly needed.

Although the CMOS process has advantages of the best solution in terms of the cost and level of integration with other functional blocks, the critical issues for CMOS PA design are the low break-down voltage and high knee voltage of the device. Most of CMOS RF power amplifiers (PAs) reported to date have been demonstrated using power-combining circuits [1] in order to reach high output power and efficiency at RF frequencies, which generally degrade the performance of CMOS PAs to narrowband and low-linearity characteristics and make them unsuitable for MBMM applications.

II. DESIGN AND RESULTS

In this paper, a stacked-FET topology using 0.11μm 1.2V standard CMOS technology is employed for the main stage to overcome various breakdown problems and to boost the output voltage swings as well as output impedance of the PA, as shown in Fig. 1 [1]. Therefore, the PA naturally owns an insensitive load matching network and also wideband characteristic. Furthermore, the output matching network controls impedances of fundamental and higher harmonics based on 'Continuous class-F' theory to increase the average efficiency [2].

In Fig. 2, the proposed amplifier achieves a saturated output power of over 27.9 dBm and a PAE of 43.3% from 1.7 GHz to 2.3 GHz, centered at 2 GHz. The two-tone test is simulated at 1.95 GHz

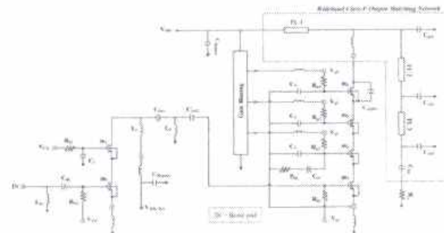

Fig. 1. Stacked-FET PA basic structure.

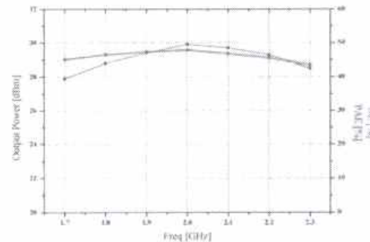

Fig. 2. Simulated DE, PAE and saturated Pout as a function of frequency.

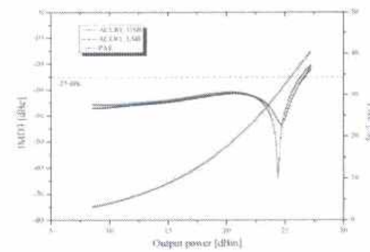

Fig. 3. Simulated IMD3 and PAE as a function of Pout.

center frequency with 5 MHz tone-spacing and the sweet spot appears at the output power of 25 dBm to achieve lower IMD3. The linear output power is 26.4 dBm with a PAE of 37.4% under the -25 dBc, as illustrated in Fig. 3.

ACKNOWLEDGEMENT

The authors would like to acknowledge the assistance and support from the Dongbu HiTek, Seoul, Korea.

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