Commercial RFSoC-Based Wideband MIMO-FMCW Radar Design with Effective Pre-distortion

Dong-Woo Kim
Department of Electrical and Computer Engineering
INMC, Seoul National University
Seoul, Republic of Korea
cb3403@snu.ac.kr

Hojung Kang
RF Development Team (S.LSI)
Samsung Electronics
Hwasung, Republic of Korea
hjkang@ael.snu.ac.kr

YongAm Son
Innovative Product R&D Group 2
Samsung Electronics
Suwon, Republic of Korea
yongam.son@samsung.com

Seongjung Kim
Department of Electrical and Computer Engineering
INMC, Seoul National University
Seoul, Republic of Korea
sjkim@ael.snu.ac.kr

Sangwook Nam
Department of Electrical and Computer Engineering
INMC, Seoul National University
Seoul, Republic of Korea
snam@snu.ac.kr

***Abstract*—The implementation of wideband multiple-input-multiple-output (MIMO) frequency-modulated continuous-wave (FMCW) radar has several issues, such as multi-channel hardware configuration, multi-channel synchronization, and high-quality chirp generation over a wide frequency band of interest. To address these issues, this study proposes a commercial RF system-on-chip (RFSoC)-based wideband MIMO-FMCW radar architecture. In addition, it presents the digital and RF hardware scheme which makes amplitude digital pre-distortion effective, resulting in a better quality of transmitting chirped and receiving de-chirped signals. Finally, 2-D imaging results obtained from the prototype demonstrate the potential of the proposed radar architecture.**

Keywords—Digital pre-distortion, MIMO-FMCW radar, RF architecture, RFSoC, wideband chirp generation

I. Introduction

Recently, wideband frequency-modulated continuous-wave (FMCW) radars have been used in various fields. For instance, short-range imaging radars adopt the multiple-input-multiple-output (MIMO) FMCW radar architecture [1]–[3] owing to its high cross-range resolution, fast data acquisition time, and relatively low-cost implementation.

At the same time, the implementation of MIMO radar demands extra efforts, as it requires multiple synchronized analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). In this case, a commercial RF system-on-chip (RFSoC) can be a solution. Xilinx's ZYNQ Ultrascale+ RFSoC integrates multi-channel high-speed DACs and ADCs into a field-programmable gate array (FPGA), which can provide excellent performance in a relatively small area with low complexity, low power consumption, and low cost. However, to make the RFSoC-based FMCW radar system to be wideband, co-design of the digital and RF system is required. In the digital system, the multiple direct digital synthesizers (DDS) are used to generate a chirp signal in parallel, and this signal is sent to the RF-DAC using serialization block [4]–[6]. Then, the chirp signal is up-converted and broadened in the RF system using frequency multipliers and mixers. It should be noted that the highly linear chirp signal generated by the digital system gets contaminated when going through the RF system. It suffers from amplitude and phase distortion over a wide frequency band. Digital pre-distortion (DPD) technique is one option to reduce the distortion at the output. However, for a wideband system that uses multiple frequency multipliers, DPD cannot effectively compensate amplitude distortion unlike phase distortion. Amplitude distortion causes impairment of the system. It can increase the sidelobe level [7]–[8]. Besides, it can also lead to spectral regrowth due to the nonlinearity of the RF devices [9] and can affect the assessment of RF exposure compliance that limits maximum transmitting RF power [10]. Therefore, an effective amplitude DPD (A-DPD) scheme is required in a wideband system using a frequency multiplication chain. This study proposes 1) a strategy for deploying the commercial RFSoC for simple MIMO-FMCW radar realization and 2) a novel digital and RF hardware architecture for effective A-DPD.

The rest of this paper is organized as follows. Section II shows the proposed system architecture and the A-DPD scheme. In Section III, the Ku-band 16TX-16RX MIMO radar prototype and the measurement results are presented. Finally, the conclusions of the study are given in Section IV.

II. Proposed System Description

The system block diagram of the commercial RFSoC-based MIMO-FMCW radar is shown in Fig. 1. The system utilizes the XCZU28DR RFSoC platform HTG-ZRF8 [11] to connect to a host PC through PCI-Express. To generate and acquire the radar signals, it uses two DACs and four ADCs out of the eight supported 14-bit DACs and eight 12-bit ADCs. These DACs and ADCs run at 3932.16 MHz and 1966.08 MHz, respectively. Along with the RFSoC platform, an RF subsystem is used to convert, transmit, and receive the RF signals. The RF subsystem consists of frequency converter (FC) module, FMCW homodyne transceiver module, and antenna array module. The FC module converts an S-band chirp signal generated by the RFSoC to a Ku-band chirp signal. This module filters unwanted spurious components generated by the DAC and up-converts the chirp signals while extending the bandwidth. The FMCW homodyne transceiver module transmits/receives the Ku-band signals and converts them to the beat signals. This module supports multi-channel data transmission and reception using a time-division

XXX-X-XXXX-XXXX-X/XX/$XX.00 ©20XX IEEE

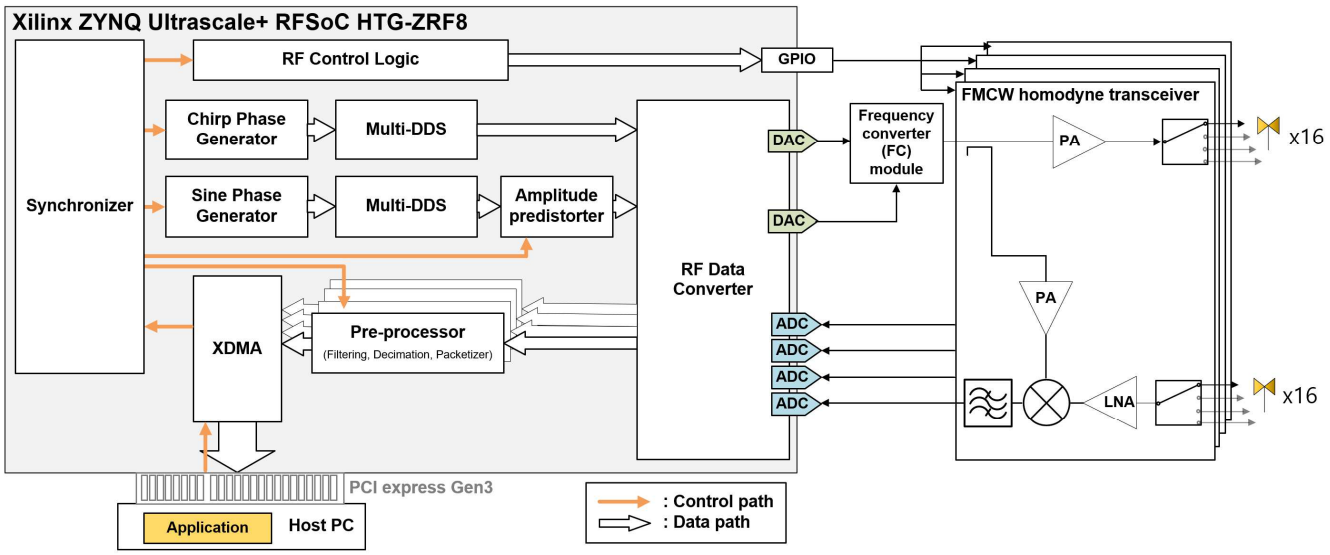


Fig. 1. Overall block diagram of the proposed commercial RFSoC-based MIMO-FMCW radar platform.

multiplexing (TDM) scheme. The antennas are connected to the SP4T switches and are turned on and off according to the TDM scheme. The system includes four transceiver modules to configure 16 transmitting and 16 receiving antennas.

A. Digital hardware and software architecture

As shown in Fig. 1, the proposed digital baseband consists of three units: 1) a transmit unit with two embedded high-speed DACs and two waveform generators, 2) a control unit with a synchronizer and RF controller, and 3) a receive unit with four embedded ADCs, four data preprocessors, and an FPGA-to-PC interface. As for the transmit unit, two multi-DDSs and DACs are used to generate chirped and sinusoidal signals. To generate the desired waveform, an adequate phase increment value per clock cycle is required. Thus, customized phase generator blocks are designed for chirped and sinusoidal signals. The amplitude predistorter is placed after the multi-DDS for the sinusoidal generator, which will be covered in Section II-B. As for the control unit, the RF control logic block supplies the RF switching control voltages. These voltages change when the chirped signal is turned off. The 1.8 V signals are sent to the transceiver modules through an FPGA mezzanine card manufactured by Future Design Systems [12]. As for the receive unit, the preprocessors are placed in parallel after the ADCs. The preprocessor comprises a decimation filter and a packetizer for data reduction and burst data transmission to the host. The stream of data packets is sent from the packetizer to the host using the PCI Express interface. Xilinx's PCIe intellectual property (IP), called XDMA, is used for implementing PCI Express Gen 3. The RFSoC is mounted on a PCIe slot of the host PC. The host PC runs on Windows 10, and Xilinx PCI Express DMA driver for Windows operating systems is used to operate the RFSoC. The application for the radar operation was written in C language and built with MinGW compiler in 64 bits.

B. Proposed wideband chirp generator architecture for effective A-DPD

A DDS-based wideband chirp generator requires the FC module in the RF subsystem to broaden and up-convert the frequency band. As shown in Fig. 2, the FC module supporting a wideband chirp generation consists of a frequency multiplier chain and down-conversion mixer [6].

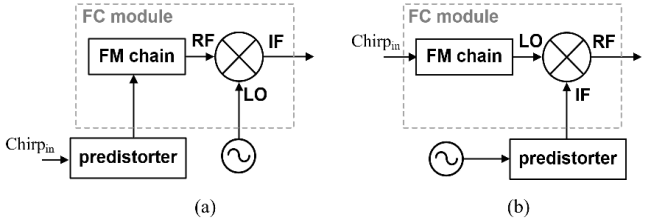


Fig. 2. Simplified block diagram of the frequency converter module and the predistorter. Frequency multiplier is abbreviated as FM in this figure. (a) Convetional scheme [6]; (b) proposed scheme

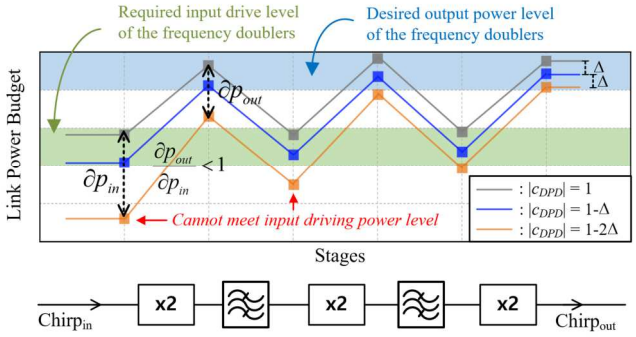


Fig. 3. Description of the A-DPD transfer reduction characteristics of the frequency multiplier chain. $|c_{DPD}|$ is the coefficient of A-DPD, where $|c_{DPD}|$ equals to one if A-DPD is not applied.

The RF subsystem, including the FC module, causes the signal distortion, so the DPD technique should be applied by designing the predistorter in the digital hardware. As shown in Fig. 2(a), the conventional scheme is to implement it on the chirp signal path; however, it is not effective in the case of A-DPD. It is due to the A-DPD transfer reduction characteristics of the frequency multiplier chain — the degree of A-DPD diminishes as it passes through each frequency multiplier — which occurs because each frequency multiplier tends to operate in saturation [13] (see Fig. 3). Accordingly, when we change the signal amplitude to some extent by applying A-DPD like the orange line in Fig. 3, the frequency multipliers

in the front stage cannot operate in saturation. Then, it will lead to a significant degradation in RF performance.

For effective A-DPD for a wideband chirp generator, this study proposes a new architecture by modifying mixer connections and arrangement of the predistorter, as shown in Fig. 2(b). The positive effects of the change in mixer connections are: 1) it can reduce AM of the chirp because mixers tend to operate with the LO in saturation; 2) the predistorter at the IF port can directly affect the output chirp. Meanwhile, we overcome the A-DPD transfer reduction characteristics by placing the predistorter at the sinusoidal signal path, which does not need the frequency multiplier chain. In summary, the proposed scheme can be realized by feeding the modulated sinusoidal signal to the IF port of the down-conversion mixer. It provides effective A-DPD results and suppresses the amplitude distortion by the frequency multiplier chain.

The coefficient for A-DPD $|c_{DPD}(t)|$ can be calculated as follows:

$$|c_{DPD}(t)| = f(t;\boldsymbol{\lambda}_1)\left(\frac{1}{|x(t)|}\right)^{\lambda_2}. \quad (1)$$

where $|x(t)|$ is the magnitude of the transmitted RF signal, $\boldsymbol{\lambda}_1$ and λ_2 are hand-tuned parameters reflecting the nonlinearity mentioned above, and $f(t;\boldsymbol{\lambda}_1)$ is a nonlinear function that can be modeled to adjust the weights for the frequency. In this paper, the modified ReLU function is used to reflect more pre-distortion at lower frequencies as follows:

$$f(t;\lambda_1) = \max\left(w_1, \frac{10-10\lambda_1}{T_p}t + 10w_1 - 9\right) \quad (2)$$

where T_p is the chirp time. Then, the amplitude pre-distorted signal $x_{ap}(t)$ can be obtained as

$$x_{ap}(t) = |c_{DPD}(t)|\, x(t). \quad (3)$$

III. Experimental Results

The RF subsystem was implemented using commercial off-the-shelf components to transmit and receive the 12 – 18 GHz signal. Specifically, a 2.5475–3.2975 GHz chirp signal was generated through the RFSoC and converted to a 20.38–26.38 GHz chirp signal after going through three frequency doublers. Then, the signal was down-converted to the Ku-band by mixing it with the 8.38 GHz sinusoidal signal. The output power of the 12–18 GHz chirp signal was measured using a spectrum analyzer to pre-distort the transmitting chirp signal. The chirp time was adjusted for tens of seconds to capture all spectra using a spectrum analyzer. The Max Hold function was used to get the magnitude of the transmitted RF signal $|x(t)|$. Then, the A-DPD coefficients can be obtained using (1). The overall process of A-DPD is illustrated in Fig. 4. The measurements were performed for two output power configurations, as shown in Fig. 5(a) and 5(b). The black lines, which are not constant over the frequency, show the output power before A-DPD. The parameters (λ_1, λ_2) for each configuration were set as (0.59, 0.57) and (0.52, 0.57), respectively. The coefficients for the length of the chirp time were obtained and stored in the block RAM and then synchronized with the sine wave and multiply them. As shown in the red lines in Fig. 5, the output signals after the proposed A-DPD have a signal strength of 7 dBm and 11 dBm over the entire Ku-band for each configuration. When the same A-

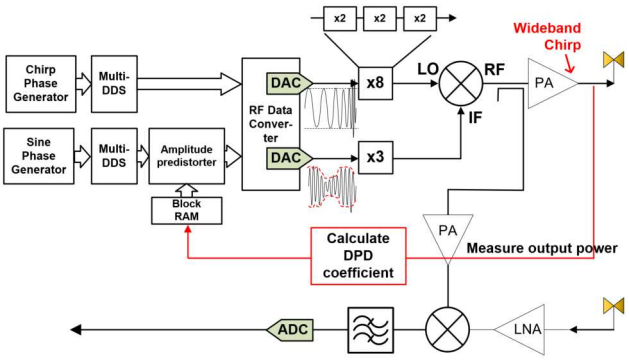
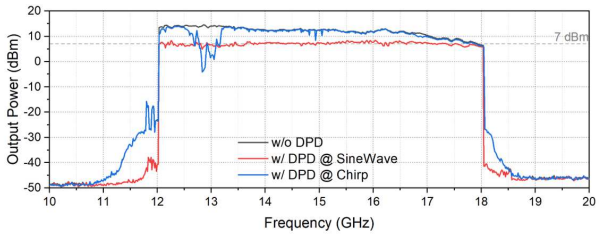
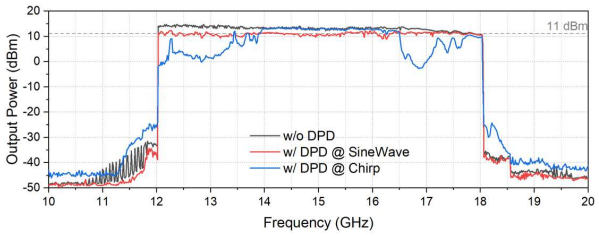


Fig. 4. Simplified block diagram of the proposed scheme for effective A-DPD. Other RF components, such as filters and attenuators, are omitted from the figure for simplicity.



(a)



(b)

Fig. 5. Measured output power over the entire Ku-band. (a) RF power configuration option 1; (b) RF power configuration option 2.

DPD coefficients were multiplied to the chirp signal, the output signals were barely changed or severely distorted, as shown by the blue lines in Fig. 5. It was due to the characteristics of the multi-stage frequency multiplier chain explained in Section II.

Based on the output chirp signal with A-DPD, the 2-D imaging was performed using a 16TX-16RX MIMO-FMCW radar prototype. The prototype was fabricated according to the block diagram in Fig. 1. As for the data acquisition scheme, a single chirp signal is transmitted over 50 μs, and 768 samples were captured with a sampling rate of 15.36 MSPS over 40 μs. To acquire all 16 TX and 16 RX channel data, the system emitted a series of chirp signals and acquired the data accordingly. Since four ADCs operated together, 3072 samples were collected simultaneously within one pulse duration and 64 chirp signals were repeatedly emitted. The total data cube size to perform 2-D imaging is 16×16×768 samples. The topology and fabricated module for the 16TX-16RX array are shown in Fig. 6. The data cubes were obtained for two cases: RF power configuration A without A-DPD (black line in Fig. 5(a)) and RF power configuration B with A-DPD (red line in Fig. 5(b)). The reason for comparing these two signals is that they have similar average power over the chirp time as 13.1376 dBm and 11.7561 dBm. They were

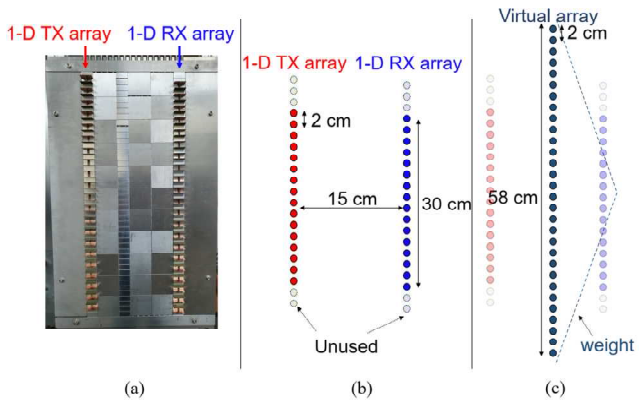


Fig. 6. 16TX-16RX MIMO array configuration; (a) photograph of the antenna array module; (b) array topology; (c) approximated virtual array

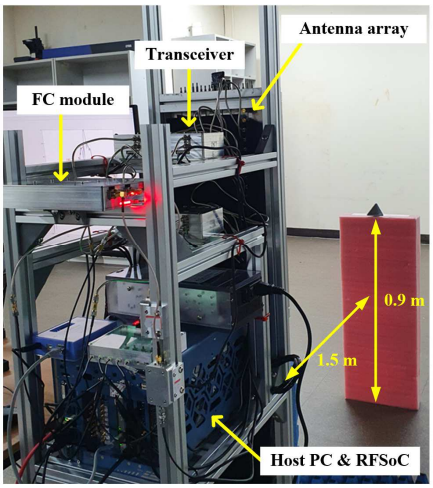


Fig. 7. Photograph of the measurement environment for near-field 2-D imaging of the corner reflector at 1.5m from the radar platform with the height of 0.9 m.

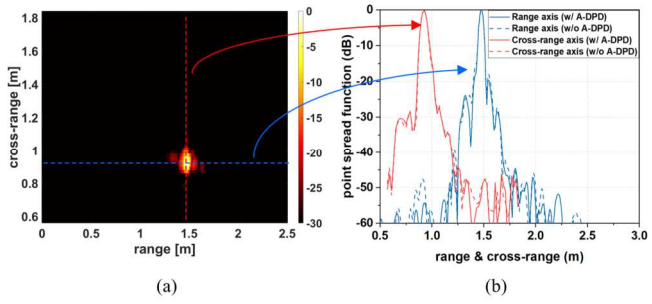


Fig. 8. Measurement results. (a) 2-D imaging with the amplitude pre-distorted chirp; (b) point spread function for the range and cross-range.

acquired for the scenario where the corner reflector is placed at 1.5 m apart from the radar platform with the height of 0.9 m. The photograph of the radar prototype and the measurement environment are shown in Fig. 7. As for the imaging algorithm, a clutter removal algorithm and the back-projection algorithm was used to reconstruct the image. As shown in Fig. 8(a), the image for the corner reflector was well reconstructed using the chirp signal with the proposed A-DPD scheme. In addition, the sidelobe characteristics were checked by comparing the point spread functions, as shown in Fig. 8(b). The sidelobe characteristics were not evidently improved when A-DPD was applied since the output signal amplitude of the prototype was not distorted enough to degrade the sidelobe level. Nevertheless, it is still worthwhile to apply A-DPD as it allows to control the transmitting RF power as intended.

IV. Conclusions

This study proposed a commercial RFSoC-based wideband MIMO-FMCW radar architecture. The strategy for deploying the commercial RFSoC facilitated the implementation of the synchronized MIMO system and DDS-based wideband chirp generation. In addition, by proposing the A-DPD scheme, the output power of a wideband chirp signal can be easily controlled as intended. Finally, the proposed RFSoC-based system architecture, including the A-DPD scheme, was verified through 2-D imaging using a 16TX-16RX MIMO-FMCW radar prototype.

Acknowledgment

This research is partially sponsored by the NATO Science for Peace and Security Programme under grant G5395 (http://www.nato.int/science).

References

[1] D. Bleh et al., "A 100 GHz FMCW MIMO radar system for 3D image reconstruction," *2016 European Radar Conference (EuRAD)*, 2016, pp. 37-40.

[2] M. E. Yanik and M. Torlak, "Near-field MIMO-SAR millimeter-wave imaging with sparsely sampled aperture data," *IEEE Access*, vol. 7, pp. 31801-31819, 2019.

[3] S. Kueppers, H. Cetinkaya, R. Herschel, and N. Pohl, "A compact 24×24 channel MIMO FMCW radar system using a substrate integrated waveguide-based reference distribution backplane," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 6, pp. 2124-2133, June 2020

[4] K.-R. Kim and J.-H. Kim, "Wideband waveform generation using MDDS and phase compensation for X-Band SAR," *Remote Sens.*, vol. 12, no. 9, p. 1431, May 2020.

[5] D. Gomez-Garcia, C. Leuschen, F. Rodriguez-Morales, J.-B. Yan, and P. Gogineni, "Linear chirp generator based on direct digital synthesis and frequency multiplication for airborne FMCW snow probing radar," in Proc. *IEEE MTT-S Int. Microw. Symp. (IMS)*, Tampa, FL, USA, Jun. 2014, pp. 1–4.

[6] J. Yan *et al.*, "Airborne measurements of snow thickness: Using ultrawideband frequency-modulated-continuous-wave radar," *IEEE Geosci. Remote Sens. Mag.*, vol. 5, no. 2, pp. 57–76, Jun. 2017.

[7] A. Laloue *et al.*, "An efficient method for nonlinear distortion calculation of the AM and PM noise spectra of FMCW radar transmitters," *IEEE Trans. Microw. Theory Techn.*, vol. 51, no. 8, pp. 1966–1976, Aug. 2003.

[8] B. Sun *et al.*, "Digital radar implementation with amplitude predistortion," *In Proc. IEEE Radar Conf.*, 2017, pp. 1691–1696.

[9] D. R. Morgan *et al.*, "A generalized memory polynomial model for digital predistortion of RF power amplifiers," *IEEE Trans. Signal Process.*, vol. 54, no. 10, pp. 3852–3860, Oct. 2006.

[10] IEC 62232:2017, "Determination of RF field strength, power density and SAR in the vicinity of radiocommunication base stations for the purpose of evaluating human exposure," Aug. 2017.

[11] HitechGlobal. HTG-ZRF8—Product Page. Accessed: Oct. 21, 2021. [Online]. Available: http://www.hitechglobal.com/Boards/Zynq_RFSoc.htm

[12] Future Design Systems. CON-FMC—Product Page. Accessed: Oct. 21, 2021. [Online]. Available: http://wiki.future-ds.com/doku.php?id=en:products:con-fmc#features

[13] W. F. Egan, *Practical RF System Design*. New York, NY, USA: Wiley, 2003.