A 77-GHz FMCW Radar System Using On-Chip Waveguide Feeders in 65-nm CMOS

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***Abstract*—This paper presents a 77-GHz radar system using a transmitter (Tx) and receiver (Rx) integrated with on-chip waveguide feeders in 65-nm CMOS. The newly proposed on-chip waveguide feeder shows the insertion loss of about 2 dB and more than 30% bandwidth. Additionally, both the Tx and Rx are integrated with internal $\times 10$ frequency multipliers. Therefore, a radar system can be easily implemented without sensitive millimeter-wave packaging technology by mounting the Tx and Rx chips on the waveguide aperture. The interconnections for the low-frequency reference and baseband signals can be realized on the low-cost FR-4 printed circuit board. The radar system shows 9-dBm output power and 13-dB down-conversion gain from the waveguide port.**

***Index Terms*—Automotive radar, CMOS, frequency multipliers, millimeter-wave (mm-wave) packaging, on-chip feeder.**

I. Introduction

RECENTLY, car radar sensors are increasingly used for avoiding critical traffic accidents, driving assistance, and finally, autonomous driving in the near future. Compared to other radars used for aerospace and military systems, car radar sensors should have small size and consume low power. More importantly, low-cost implementation is essential to be equipped even in compact cars. Recent development of long-range radar systems at 77 GHz is mainly based on the SiGe technologies with planar packaging using low-loss substrates [1]. Considering the level of integration, power consumption, and manufacturing cost for mass production, the CMOS technology seems to be an alternative solution since the continued development of CMOS technology successfully demonstrates its millimeter-wave (mm-wave) applications for 60-GHz wireless data link and 77-GHz automotive radar systems [2]–[7].

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The mm-wave frontend of radar system requires high performance, high level of integration, low power, and low manufacturing cost. The main challenge for CMOS technology compared to SiGe is the performance. A comparison of CMOS and SiGe technologies for car radar applications can be found in [8]. Advanced CMOS technology is essential to meet the f_T, f_{MAX} requirements for mm-wave design. The noise performance, especially the phase noise and $1/f$ noise, is another challenge because of the homodyne structure of frequency-modulated continuous-wave (FMCW) radar system.

In general, the CMOS process shows poorer phase-noise and flicker-noise performance than the SiGe process. However, with advanced design methods, the CMOS voltage-controlled oscillator (VCO) showed improved phase-noise performance of -95 dBc/Hz at 1-MHz offset from 90.3 GHz using a Colpitts quadrature VCO [9] and -109 dBc/Hz at 10-MHz offset from 77 GHz using high-Q coplanar-waveguide (CPW) transmission-line tank [10]. An alternative solution for good phase noise is the frequency multiplier based synthesizer [11]–[16]. Phase noise of multipliers mainly relies on reference phase noise. The reported phase-noise characteristics at 1-MHz offset are about -108 dBc/Hz at 93 GHz using a frequency tripler and an external source [14], -110 dBc/Hz at 78 GHz using a $\times 10$ frequency multiplier and an external source [15], and -93 dBc/Hz at 96 GHz using an integrated tripler and phase-locked loop (PLL) [16].

Besides the challenges from the current CMOS technology, packaging is a critical issue in mm-wave systems regardless of the technologies. The most popular technique is the planar packaging using the wire or flip-chip bonding. The wire bonding requires careful control of the wire bonds and a low-loss substrate to reduce the transition loss. The flip-chip packaging shows excellent RF performance [1], [17]. However, the cost and the manufacturing complexity are increased. To avoid the high cost, loss, and sensitivity of packaging for silicon mm-wave systems, on-chip antennas have been developed [18], [19]. However, their gain and efficiency are not sufficient for long-range sensing and communications.

This work focuses on finding the solution to circumvent the sensitive packaging and improve phase noise of CMOS mm-wave systems. This work presents a frequency multiplier based 77-GHz CMOS radar transmitter (Tx) and receiver (Rx) with improved phase noise. In addition, this work proposes a novel on-chip waveguide feeder on silicon substrate, which enables the easy integration of radar systems free of mm-wave packaging issues. The proposed radar system is composed of

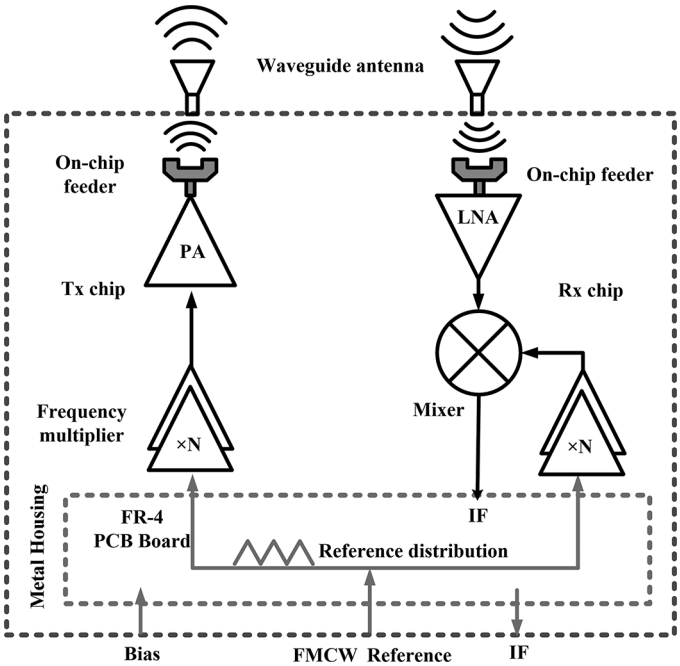


Fig. 1. Proposed FMCW radar architecture.

separate Tx and Rx chipsets operating at 77 GHz, as shown in Fig. 1. The Tx consists of a power amplifier (PA), $\times 10$ frequency multiplier, and on-chip waveguide feeder. The Rx includes a low-noise amplifier (LNA), down-conversion mixer, $\times 10$ multiplier, and on-chip waveguide feeder. The on-chip waveguide feeders are directly mounted on the waveguide apertures without additional interconnects. Therefore, the signal of the highest frequency requiring wire interconnects to the external world is the reference signal at 7.7 GHz.

To implement the proposed system, the Tx and Rx chipsets are designed using a 65-nm low-power RF CMOS process with 1-poly 9-metals. NMOS field-effect transistors (FETs) of the process biased at 250-μA/μm current density show f_T and f_{MAX} of 126 and 225 GHz, respectively.

This paper is organized as follows. In Section II, details about the design of the on-chip waveguide feeder and electromagnetic (EM) simulation results are presented. In Section III, designs of the frequency multiplier, and the Rx and Tx chipsets with the on-chip feeders are explained. Measurement results of the designed chipsets and modules will be shown in Section IV. The radar system implementation and its experimental results will be presented in Section V followed by a conclusion in Section VI.

II. Design of On-Chip Waveguide Feeder

The proposed on-chip waveguide feeder is composed of an E-plane waveguide probe and two quarter-wave open stubs on the chip ground plane. These parts are integrated on a silicon substrate to directly feed the external high-gain antennas, such as waveguide horn or waveguide slot array antennas without additional mm-wave interconnects.

The on-chip rectangular waveguide feeders have been developed for compound monolithic microwave integrated circuits [20], [21]. However, their development required thru-wafer vias from the chip ground to the waveguide wall and additional back

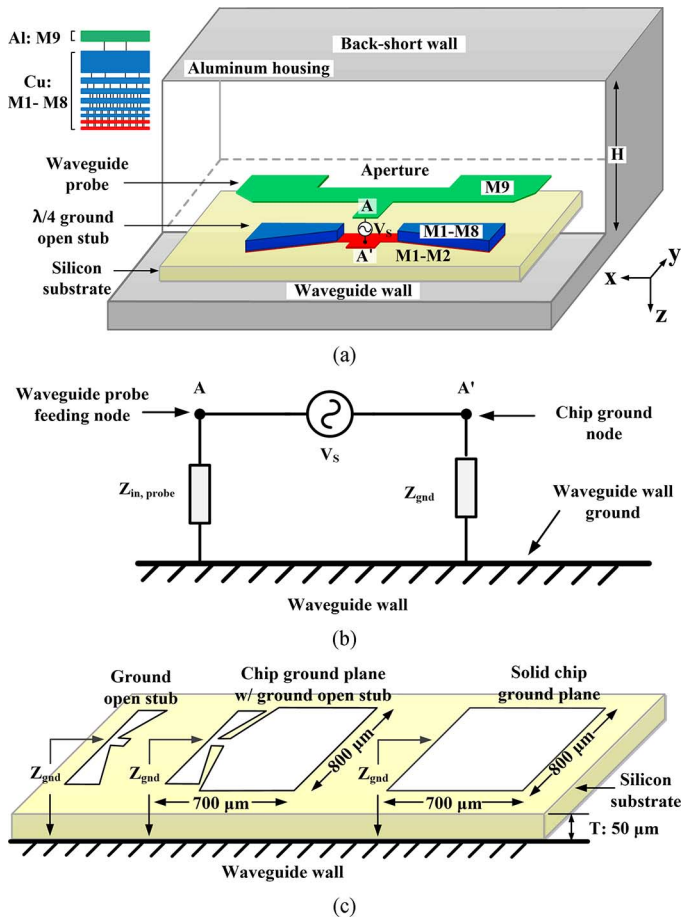


Fig. 2. Proposed on-chip waveguide feeder. (a) 3-D view and metal layers. (b) Electrical equivalent circuit of the proposed waveguide feeder. (c) Three simulation structures to compare the impedance Z_{gnd}.

metallization, which are not available in the standard CMOS process. Instead of the thru-wafer vias, this work introduces the segmented quarter-wave open stub on the chip ground plane in the silicon substrate. This composes the microstrip line mode on the waveguide wall and provides the contactless shorting path to the waveguide wall from the chip ground. The proposed on-chip feeder for the WR-10 waveguide is shown in Fig. 2. The feeder is directly mounted on the waveguide aperture with a back-shorting metal block. Theoretically, the back-short should be placed at $\lambda_g/4$ above the feeder, where λ_g is the guided wavelength in the waveguide. In practice, the height H of the back-short location and the dimensions of the waveguide probe are adjusted to achieve the impedance matching. The metal layers used in the design are shown in Fig. 2(a). The top aluminum layer is used for the probe and the feeding line because better return loss is obtained than the case of using the thick copper layer. Two lowest stacked metal layers form the chip ground plane of the active circuit design, as shown in Fig. 2(a). The ground open stub uses entire metal layers to reduce the metallic loss. The electrical equivalent circuit of the proposed waveguide feeder is given in Fig. 2(b). The system ground reference is formed on the waveguide wall. The impedance Z_{gnd} is the grounding impedance through wafer between the chip ground node and waveguide wall ground. The impedance $Z_{\mathrm{in,probe}}$ is the input

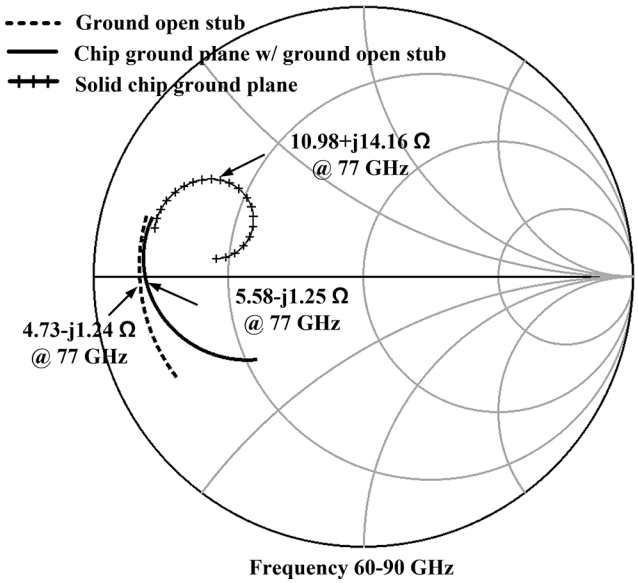


Fig. 3. Simulation results of $Z_{\rm gnd}$ between chip ground node and waveguide wall ground.

impedance seen by the probe between the probe feeding node on the chip and the waveguide wall. The $\lambda/4$ ground open stub guarantees low $Z_{\rm gnd}$ regardless of the size of the chip ground plane. To confirm the effectiveness of the ground open stub, EM simulations for three cases were performed with a port between the chip ground node and the waveguide wall, as depicted in Fig. 2(c). According to the simulation results shown in Fig. 3, the ground open stub successfully provides a low-impedance path to the waveguide wall at 77 GHz, as expected. The thru-wafer impedance hardly changes even with the chip ground plane, whereas the solid chip ground plane without the stub shows much higher inductive impedance, which severely changes depending on the dimension of the solid chip ground plane. The nonzero resistive impedance of the ground open stub is mainly due to the conductivity of the silicon substrate and it introduces about 0.4-dB transition loss for feeder operation assuming an ideal lossless 50-Ω probe.

A U-shaped E-plane waveguide probe is devised to reduce the probe length for saving the die area and achieve an effective wideband matching. As shown in Fig. 2(a), the ground open stub is parallel to the bottom section of the U-shaped probe, which ensures the return current to mostly flow through the open stub rather than back-spread to the wide chip ground plane. The top and side views are shown in Fig. 4(a) and (b) with detailed dimensions. The bottom of the silicon substrate of the feeder faces the forward direction of the waveguide. To minimize the substrate loss, the substrate is thinned to 50-μm thickness, which still maintains the mechanical ruggedness of the wafer.

3-D EM simulation was carried out to estimate the performance of the proposed on-chip feeder. As shown in Fig. 4(b), one port is at the on-chip feeding point (Port 1) and the other port is placed 5 mm away from the feeder at the waveguide side (Port 2). The insertion loss from Port 1 to Port 2 is 1.37 dB at 77 GHz, as shown in Fig. 5. The input return losses at Port 1 and Port 2 are better than 15 dB from 60.3 to 90.4 GHz with 30.1-GHz bandwidth (BW), and from 62 to 97.3 GHz

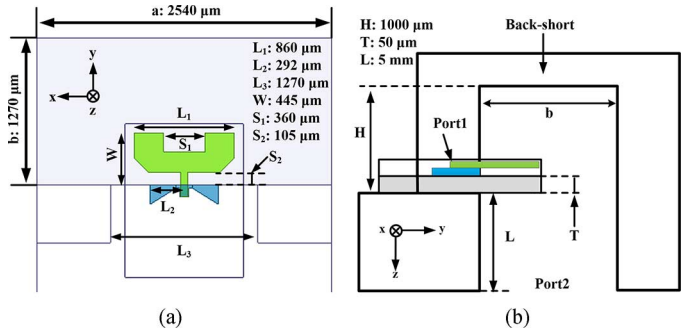


Fig. 4. Proposed on-chip waveguide feeder. (a) Top view in xy-plane. (b) Side view in yz-plane.

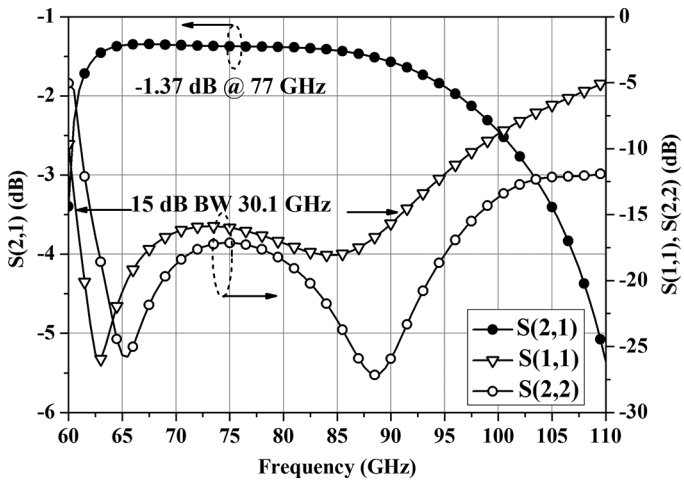


Fig. 5. S-parameter simulation results of the on-chip waveguide feeder using 3-D EM simulator.

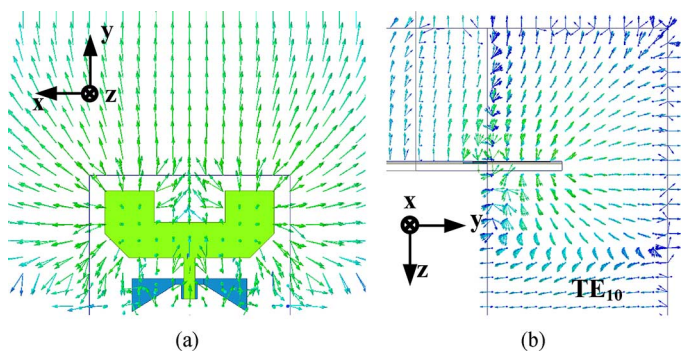


Fig. 6. E-field distribution in: (a) xy-plane and (b) yz-plane.

with 35.3-GHz BW, respectively. The wideband matching is achieved without additional matching circuitry. In case of a lossless silicon substrate, the insertion loss of the proposed feeder is reduced to 0.36 dB. Fig. 6 shows the electric field distribution in the xy-plane and yz-plane, which confirms that the $\rm TE_{10}$ transmission mode is successfully excited.

Concerning the assembling tolerance for the position of the die attach, EM simulations were performed with various chip positions within 50-μm misalignment in all directions. Simulation results show that misalignment along the x-direction [see Fig. 4(a)] increases the insertion loss less than 0.1 dB. For the change in the forward y-direction, the insertion loss increases

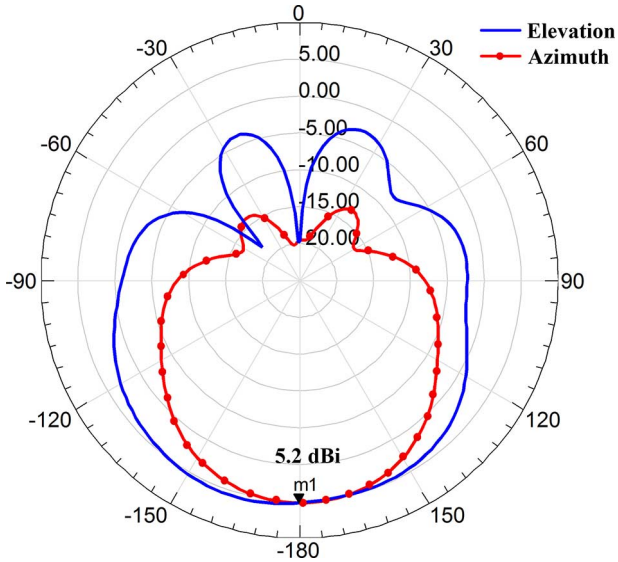


Fig. 7. Simulation results of radiation patterns of WR10 aperture fed by the proposed on-chip feeder. The length of the waveguide is 1 mm. Elevation pattern (E-plane), azimuthal pattern (H-plane).

less than 0.2 dB. However, moving backward in the y-direction causes a 0.4-dB increase because it changes the probe length with respect to the ground wall of the waveguide. Therefore, the chip should be carefully mounted so that the space S_2 in Fig. 4(a) is not overlapped on the waveguide flange.

The proposed on-chip waveguide feeder can be used with and without external antennas depending on the required gain for system implementation. When only the waveguide aperture is used as an antenna, an ideal TE_{10} mode excitation gives the gain of 6.5 dBi according to EM simulation. However, due to the loss of the on-chip feeder, the gain of the aperture antenna driven by the proposed feeder shows the reduced gain of 5.2 dBi, as confirmed by the simulation results in Fig. 7. Nonetheless this result indicates that the proposed feeder on the conducting package with a rectangular aperture can be used as an antenna as it is. This configuration can be a very low-cost solution for short-range radar sensors for side-looking or short-range wireless data link systems.

Since back-to-back measurements of the proposed feeders are not plausible due to its short length, we designed the 77-GHz Tx and Rx with and without on-chip feeders to confirm the performance of the proposed feeder. The measurement results and the comparison with and without feeders will be given in Section IV.

III. Design of Frequency Multiplier, Rx, and Tx

A. Frequency Multiplier Design

As we explained in Section I, the frequency multiplier is adopted instead of PLLs for local oscillator (LO) signal generation because of its better phase noise and smaller size. The reproduced block diagram of the $\times 10$ frequency multiplier is shown in Fig. 8, which was published in [15]. The $\times 10$ frequency multiplier is composed of a single-to-differential (STD) converter, differential five-phase injection-locked ring oscillator

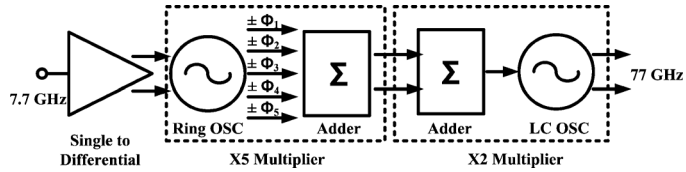


Fig. 8. Block diagram of $\times 10$ frequency multiplier.

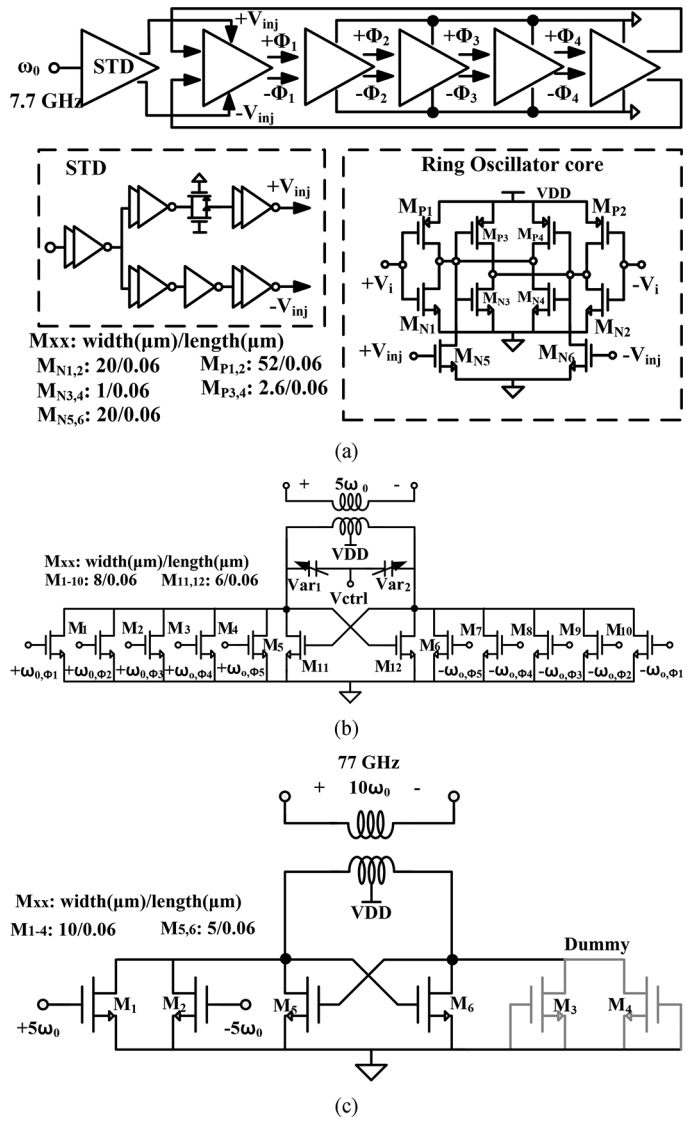


Fig. 9. Schematic of $\times 10$ frequency multiplier. (a) STD circuitry and ring OSC. (b) Five-push frequency adder. (c) Push–push frequency doubler.

(OSC), five-push adder, and push–push doubler. The schematic is shown in Fig. 9.

The input reference is converted to the differential signal through the inverter-based STD circuitry, as shown in Fig. 9(a).The free-running operating frequency of the ring OSC is set to 7.7 GHz. The differential reference signal is injected into one of the ring OSC cells shown in Fig. 9(a) and the injection-locked five differential signals with $2\pi/5$ phase offset at 7.7 GHz are obtained. The 7.7-GHz voltage signals with rich harmonic components from the ring OSC are combined in the current domain by the following adder stage. The adder is a

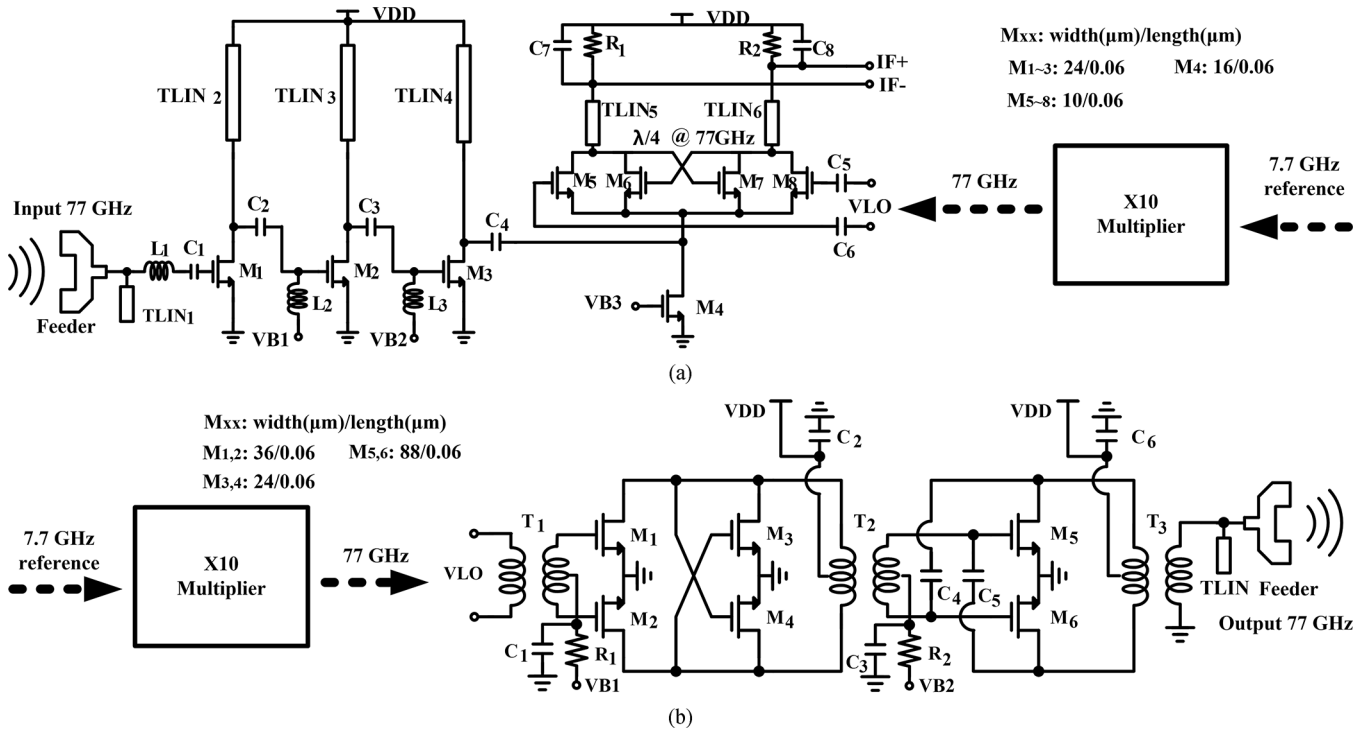


Fig. 10. Frequency multiplier based Tx and Rx with on-chip feeders. (a) Rx with an on-chip feeder. (b) Tx with an on-chip feeder.

common-source (CS) differential amplifier sharing the output load, as shown in Fig. 9(b). Assuming the linear operation of the adder, the harmonic currents are combined at the common output of the adder. In principle, due to the phase relation of the fundamental and the harmonic currents, only the harmonic currents of fifth and higher orders are constructively added and other lower harmonic currents are canceled out [12].

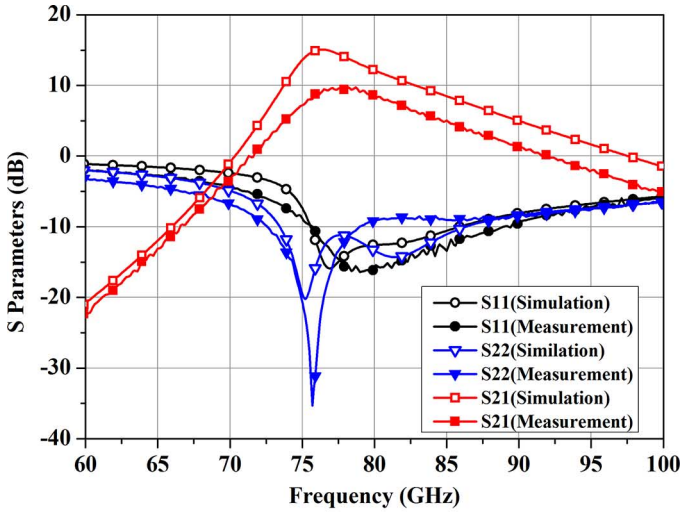
For an ideal ring OSC output, the combined harmonic components at the output of the adder generate the magnitude as large as that of the fundamental signal. However, in practice, they are attenuated due to the low-pass nature of active devices for both of the ring OSCs and adder amplifiers. Additionally, asymmetry caused by the injection cell in the ring OSC results in uneven skew of the multi-phase output of the ring OSC, which causes the unwanted spurious signals. Therefore, although the large number of ring OSC stages is preferred for higher multiplication ratio, the number of the stage should be carefully selected considering the magnitude and spurious signal generation. The strength of the fifth harmonic component is inherently enforced by adequately biasing the adder amplifier. In theory, the fifth harmonic current components of class-A and class-B amplifiers are zero, but the class-AB operation produces a nonzero fifth harmonic current [22]. Therefore, the class-AB-biased adder amplifier helps to enhance the fifth-harmonic component. The fifth harmonic is additionally boosted by the cross-coupled pair and the resonant load. The resonant load also rejects the unwanted harmonics and spurs due to the phase and amplitude mismatch. Therefore, only the desired 38.5-GHz signal can be coupled through the transformer to the push–push doubler. The push–push doubler is implemented by tying the drain nodes of the differential CS pair and loading this node with a second harmonic resonant tank composed of the transformer, as shown in Fig. 9(c). The second harmonic signal generated at the common node is injected into the injection-locked OSC to obtain the differential output signal. Dummy cells are used to improve the output balance.

There is a tradeoff between the lock BW and the output swing depending on the quality factor of the *LC* tank for both multiplier stages. With the high quality factor, the high output swing is obtained at the cost of lock BW.

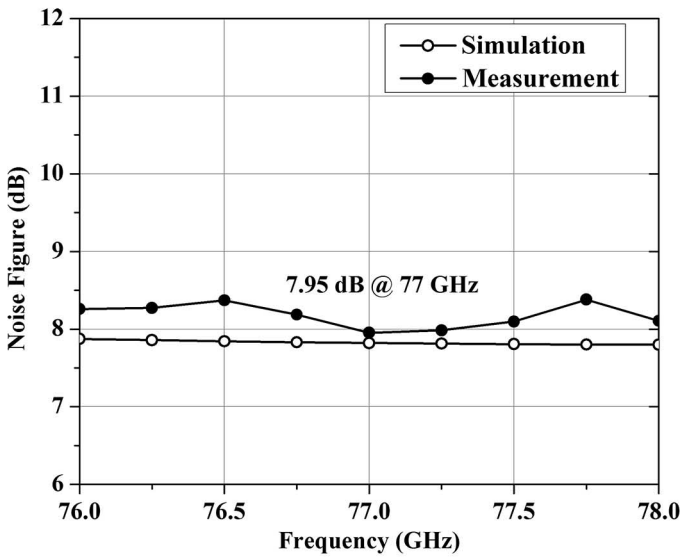
B. Rx Design

The LNA and the mixer in Fig. 10(a) are based on the work demonstrated in [23]. The LO signal $V_{\rm LO}$ for the mixer is driven by the $\times 10$ multiplier integrated in the Rx. The on-chip feeder is directly attached to the input of the LNA. The LNA consists of three-stage CS amplifiers. Two lowest metal layers are stacked as ground plane and 3-μm-thick top copper and 1.3-μm-thick aluminum layers are stacked as the signal line. The signal line is 4.6 μm wide and 3.8 μm above the ground plane. The transmission line has 32-Ω characteristic impedance and 2-dB/mm insertion loss. The transmission line $\rm TLIN_1$ and the inductor L_1 are used for the input matching. The inductors L_2 and L_3 are used for inter-stage matching and $\rm TLIN_2$, $\rm TLIN_3$, and $\rm TLIN_4$ work as loads. On-wafer measurement results of the LNA alone are given in Fig. 11. The peak gain is 10 dB and the noise figure (NF) is 7.95 dB at 77 GHz, consuming 22.8 mW. The measured gain is far less than the simulated one. Considering the correspondence between the resonant frequencies, it is considered that the uncounted degeneration inductance of the CS stage seems to be the main cause of gain reduction.

The high-gain mixer with low LO power using a split self-driven switching cell [24] is used as a down-conversion mixer. The use of the split cross-coupled switching cell can reduce the

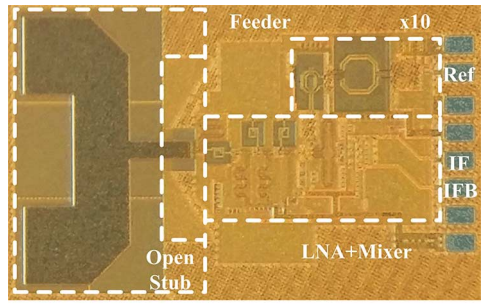


(a)

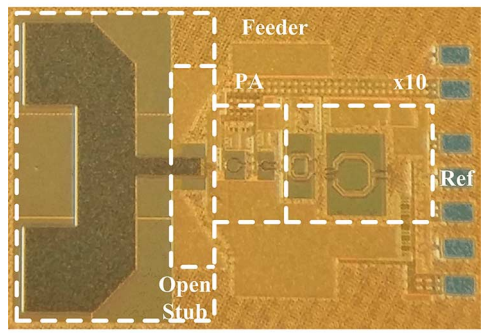


(b)

Fig. 11. On-wafer measurement results of the standalone LNA. (a) S-parameters. (b) NF.



(a)



(b)

Fig. 12. Die micrographs. (a) Rx chip. (b) Tx chip.

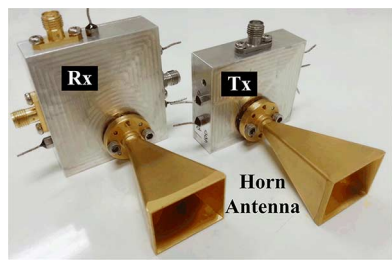


Fig. 13. Rx and Tx modules.

required LO power and enhance the gain. The output current from the LNA is directly applied to the mixer switching core. The input parasitic capacitance of the mixer is resonated by the load of the LNA. Therefore, the chip size and the layout complexity are significantly reduced because no additional inductor is required to neutralize the parasitic capacitance at the tail of the switching stage. The die micrograph of the Rx with the feeder is shown in Fig. 12(a). The Rx chip occupies 0.91 mm $\times$ 1.46 mm area including the on-chip feeder. The Rxs with and without the feeders were fabricated for comparison. The measurement results will be given in Section III-C.

C. Tx Design

The frequency multiplier based Tx with the on-chip feeder is shown in Fig. 10(b). The 77-GHz output signal of the $\times 10$ frequency multiplier is coupled to the PA by a transformer. The PA is designed using two-stage CS amplifiers [23]. The first stage includes a cross-coupled pair structure to obtain a high-voltage swing with low power consumption and reduce capacitive loading of the frequency multiplier. The second stage employs the cross-coupled neutralization capacitance between the gate and the drain to improve the stability as well as the gain [25]. Transformers are used for the impedance matching and the coupling for both stages. The output of the PA is directly connected to the on-chip feeder. The same on-chip feeder used in the Rx is attached to the output of the PA without additional tuning. As shown in Section II, the input impedance of the feeder was matched to 50 Ω for wide BW. The transformer T_3 and the TLIN are used to transform 50-Ω load impedance to an optimum impedance.

The performance of the PA alone can be referred to the previous work [23]. The PA has a gain of 8.5 dB and output power of 9.6 dBm at saturation. The peak power-added efficiency (PAE) is 6.45% and dc power consumption is 112 mW. The die micrograph of the Tx chip with the on-chip feeder is shown in Fig. 12(b). The Tx chip occupies 0.91 mm $\times$ 1.36 mm area including the on-chip feeder. The frequency multiplier based Tx with the on-chip feeder and the one without the feeder were assembled for comparison and the results will be given in Section IV.

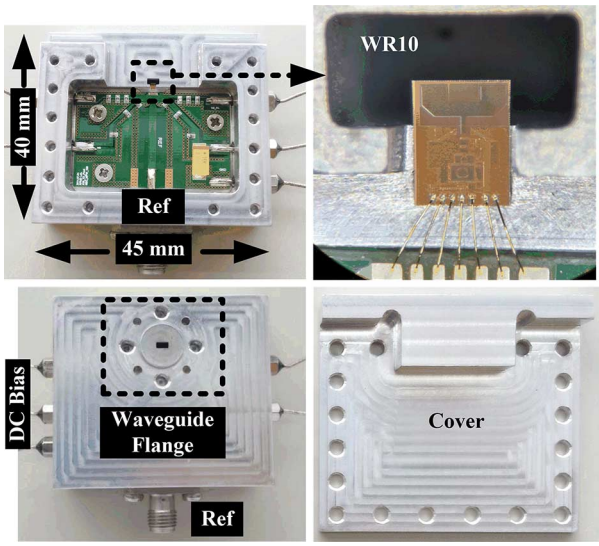


Fig. 14. Fabricated Tx module with an on-chip feeder mounted on the aperture.

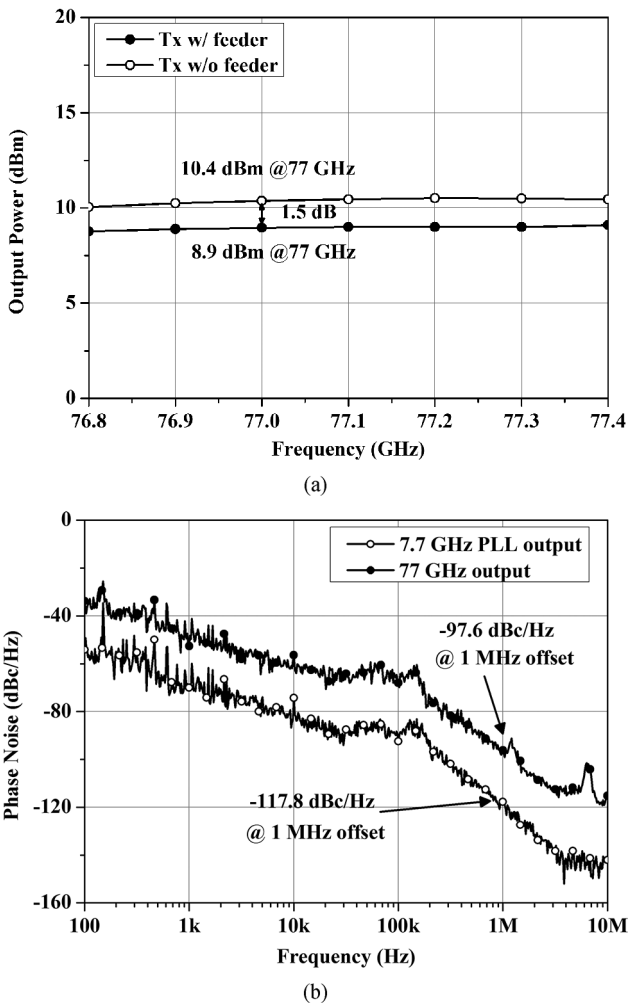


Fig. 15. Tx module measurement results. (a) Output power. (b) Phase noise.

IV. FMCW Radar System Implementation

The Tx and the Rx modules were implemented using the chips designed in the previous sections. An FMCW radar system was simply built using these two modules, commercial horn antennas, and an external signal generation module following the configuration in Fig. 1. The horn antennas can be easily mounted at the apertures of the modules. The assembled modules with 24-dBi horn antennas are shown in Fig. 13.

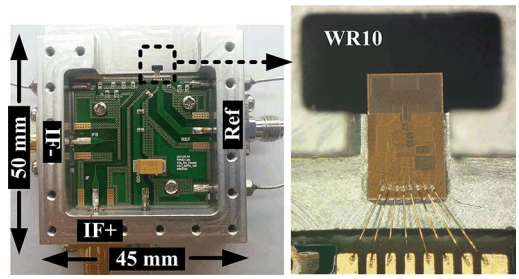


Fig. 16. Fabricated Rx module with an on-chip feeder mounted on the aperture.

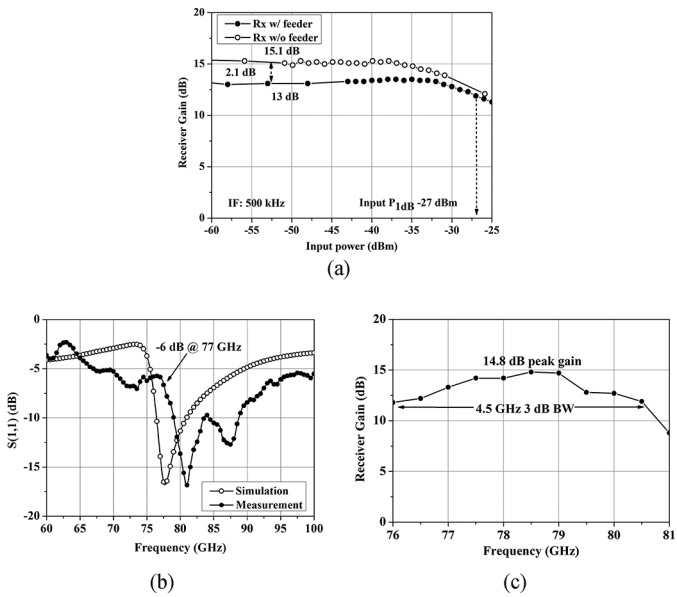


Fig. 17. Rx module measurement results. (a) Conversion gain with and without feeder. (b) Input return loss. (c) Measured conversion gain.

A. Tx Module

The Tx module using the developed chip is shown in Fig. 14. The aluminum metal housing is used to build WR10 waveguide and attach the chip. The chip is directly mounted on the waveguide aperture to feed the 77-GHz signal. The other side of the aperture is a standard UG-387/U waveguide flange to connect the horn antenna. The back-short of the waveguide is realized using the metal cover. The reference signal and the dc bias are distributed using the low cost FR-4 printed circuit board (PCB) and low-frequency wire bonding. The PCB is installed inside the metal housing. The reference signal is applied to the module through an SMA connecter. The dimension of the module is 4 cm $\times$ 4.5 cm $\times$ 1.4 cm.

The signal generator model HP 8340B is used to provide a 7.7-GHz reference signal of 0-dBm power to test the Tx module. The Tx chip without the on-chip feeder is measured using on-wafer probing. The measurement results of the Tx module with and without the on-chip feeder are shown in Fig. 15. The module achieves 8.7–9.1-dBm output power within a 76.8–77.4-GHz lock range. The output power is 1.5 dB lower

TABLE I
COMPARISON OF TRx PERFORMANCE

	[2]	[3]	[4]	[5]	[6]	This Work
Function	VCO based TRx	PLL based TRx	PLL based TRx	PLL based TRx	PLL based Tx	Multiplier based Tx, Rx
Technology	90 nm CMOS	90 nm CMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS
FMCW Generation	External VCO control	External DDFS	Fractional-N	Fractional-N	Fractional-N	External DDFS and PLL
Frequency (GHz)	73.5-77.1	78.1-78.8	75.6-76.3	76.0-76.7	76-81	76.8-77.4
Phase Noise (dBc/Hz @ 1MHz offset)	-86	-85	-85.33	-85	-83.43	-97.6
Tx Output Power (dBm)	3.3-6.3	-2.8	5.1	6.4	3	8.9
PA Power Gain (dB)	-	14	13.7	15.1	-	8.5
Rx Conv. Gain (dB)	2±1.5	23.1	38.7	23	-	13
LNA NF (dB)	6.8	15.6 (1)	7.4	14.8(1)	-	7.95
Max. Measured Distance (m)	-	8	106	-	-	85.2
Power Consumption (mW)	920	520	243	275	320	Tx 264.4, Rx 203
Chip Area (mm^2)	2.4×1.2	3.5×1.95	0.95×1.1	1.03×0.94	1.48×1.85	Tx 0.91×1.36, Rx 0.91×1.46

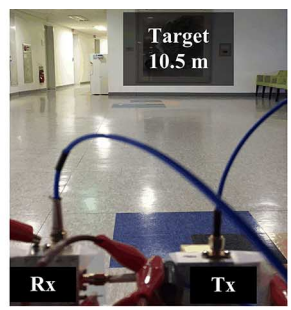
(1) Receiver noise figure.

than that of the on-wafer measurement of the chip without the feeder. The output power of the Tx seems to be saturation power considering the separate PA measurement results [23]. The loss is close to the value of the on-chip feeder simulation result in Fig. 5. The phase noise of the 77-GHz output signal measured at the waveguide output is −109.1 dBc/Hz at 1-MHz offset frequency. The phase noise of the 7.7-GHz reference signal is −132.3 dBc/Hz at the same offset. The dc power consumption of the Tx module is 264.4 mW.

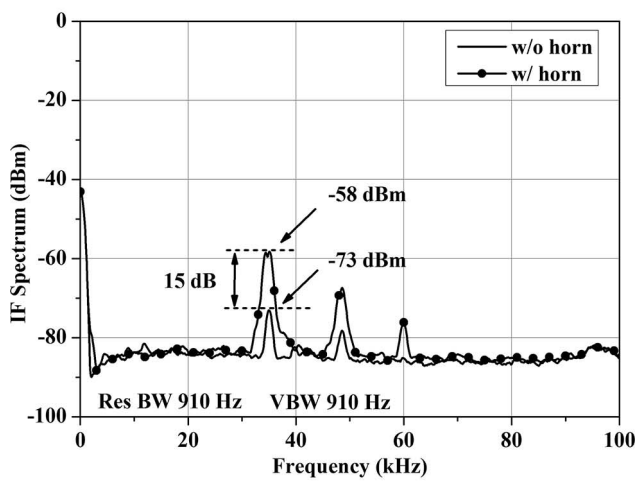
B. Rx Module

The Rx module is shown in Fig. 16. The chip is also directly mounted on the waveguide aperture. The other side of the aperture and the metal cover are the same as those of the Tx module. The reference signal, the dc bias, and the IF signals are distributed using the FR-4 PCB. The dimension of the module is 5 cm × 4.5 cm × 1.4 cm.

For gain measurement, the waveguide input port of the Rx module is driven by the W-band signal from the ME7838A vector network analyzer (VNA) and the external signal generator provides 7.7-GHz reference with 0-dBm input power. The IF signal is measured using the Agilent N9030A signal analyzer. For comparison, the Rx chip without the on-chip feeder is measured using on-wafer probing. The measurement results of the Rx module with and without the on-chip feeder are shown in Fig. 17(a). The module achieves 13-dB gain at 77 GHz, which is 2.1 dB lower than that of the chip without the feeder. The input return loss measured at the waveguide aperture shows frequency up-shift and $S11$ is −6 dB at 77 GHz, as shown in Fig. 17(b). The impedance mismatch will lead to additional 0.8-dB loss compared to the well-matched condition. Taking into account the mismatch loss, insertion loss of the feeder itself is close to the simulation result in Fig. 5. The Rx gain with different RF frequencies also shows the frequency shift. As shown in Fig. 17(c), the module has 14.8-dB peak gain at around 79 GHz and 3-dB BW of 4.5 GHz for RF input. The Rx NF is roughly estimated using the spectrum analyzer by measuring the average noise power with 50-Ω waveguide termination at the RF input. The measured system NF is 41 dB at 1 MHz. The estimated flicker corner frequency is larger than 10 MHz and so the system suffers from large flicker noise. The dc power consumption of the Rx module is 203 mW. A comparison of the performance with published single-channel CMOS transceivers (TRxs) and Tx for 77-GHz FMCW automotive radar is given in Table I.



(a)



(b)

Fig. 18. In-door range detection measurement results. (a) Experiment environment. (b) Measured IF spectrum with the target 10.5 m away.

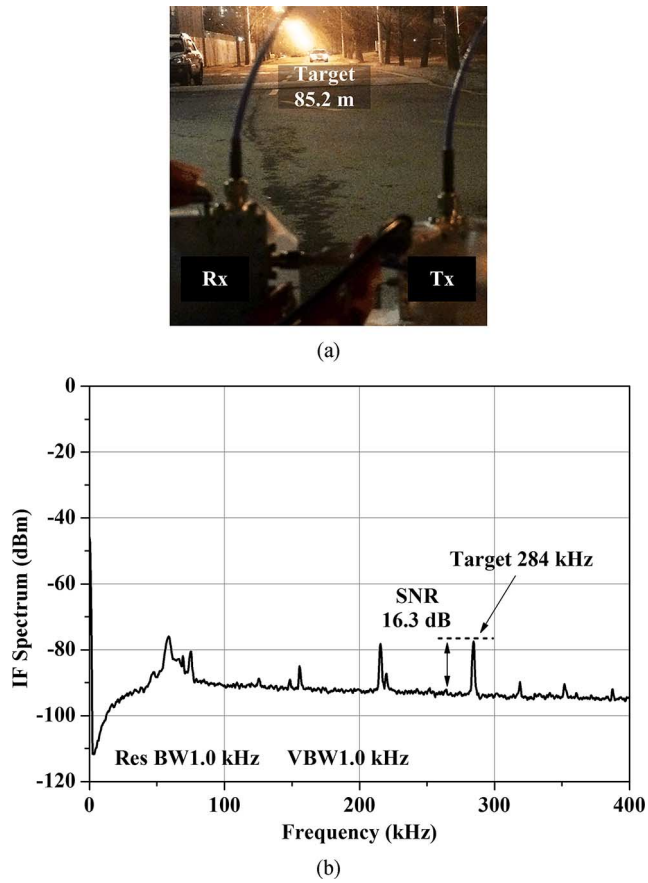


Fig. 19. Outdoor range detection measurement results. (a) Experiment environment. (b) Measured IF spectrum with the target 85 m away.

V. System Results

The radar system is tested by the range detection measurement. The Rx and Tx modules are located about 50 cm above the ground surface considering the height of the installation in the car. For the FMCW implementation, an accurate chirp reference signal generation is required. An external module composed of the Analog Device AD9958 direct digital frequency synthesizer (DDFS) and the 7.7-GHz Hittite HMC764LP6CE PLL operating in the integer mode is used to obtain the reference chirp signal with 50-MHz BW and 1-ms ramp time. The DDFS generates FMCW waveform at 50 MHz and the signal is used as the reference for the 7.7-GHz PLL. The final transmitting FMCW signal has 500-MHz BW and 1-ms ramp time, which leads to the range resolution of 30 cm. The PLL phase noise is −117.8 dBc/Hz at 1-MHz offset and the 77-GHz Tx output achieves −97.6-dBc/Hz phase noise. For the Rx measurement, the signal analyzer was used as an IF detector for the test.

At first, in-door measurement was performed using one of the differential IF output signals of the Rx, as shown in Fig. 18(a). The target was the wall 10.5 m away from the radar and the beat frequency should be 35 kHz accordingly. Although multi-targets were detected, as shown in Fig. 18(b), we can determine the echo signal from the target by analyzing the frequency and the power level. The highest power was observed at 35 kHz, as expected. The signal power was −73 dBm only with the aperture antenna. When the high gain horn antenna was attached to the Rx module, the signal power was increased by 15 dB to −58 dBm. Though the in-door environment is not anechoic for accurate comparison, the result may confirm that the gain of the simple aperture antenna is higher than 5 dBi, as explained in Section II.

The range detection in the outdoor environment was performed where a sedan served as a target, as shown in Fig. 19(a). An external 1:1 transformer with 30-kHz–70-MHz BW was used to combine the differential IF output signals for the single-ended input of the signal analyzer. The measured IF signal and the corresponding signal-to-noise ratio (SNR) are shown in Fig. 19(b). It was clearly observed that the frequency of the echo signal from the target changed as the car was moving. As specified in [26], 16-dB SNR was used for determining the maximum detectable range. We measured the echo signal with the SNR above 16 dB at 284 kHz with 1-kHz resolution BW and this corresponds to the distance of 85.2 m. The other signals in Fig. 19(b) remained unchanged as the target was moving and therefore appeared to be reflected from the standing-still objects on the sides of the road. The roll-off of the noise floor spectrum around dc is due to the BW limitation of the IF transformer.

VI. Conclusion

This work has proposed 77-GHz CMOS Tx and Rx chipsets equipped with the on-chip waveguide feeders. Using the designed chipsets, a radar system can be simply implemented without complex mm-wave packaging issues. Though the single-channel application is demonstrated, the number of channels for array radar systems and data TRxs can be easily expanded with good isolation between channels. For short-range applications, a simple aperture array on a conducting wall can configure array TRxs using the proposed on-chip feeder. When the large antenna gain is essential, a waveguide slot array antenna directly fed by the proposed on-chip feeder can be a solution. Cost and mass-production issues to implement the multi-channel system using metallic waveguide slot array antennas are expected to be solved by virtue of the recent development of cost competitive slot-array antenna systems using diffusion bonding [27], electroforming [28] or completely PCB-based post-wall slot array systems with aperture feeding capability [29]. Wide BW nature of the on-chip feeder can also be utilized for high-speed data TRxs in mm-wave applications.

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