A Fast RSSI using Novel Logarithmic Gain Amplifiers for Wireless Communication

Sungho Lee, Yonghoon Song, and Sangwook Nam

***Abstract*—This paper presents a fast received signal strength indicator (RSSI) circuit for wireless communication application. The proposed circuit is developed using power detectors and an analog-to-digital converter to achieve a fast settling time. The power detector is consisted of a novel logarithmic variable gain amplifier (VGA), a peak detector, and a comparator in a closed loop. The VGA achieved a wide logarithmic gain range in a closed loop form for stable operation. For the peak detector, a fast settling time and small ripple are obtained using the orthogonal characteristics of quadrature signals. In 0.18-μm CMOS process, the RSSI value settles down in 20 μs with power consumption of 20 mW, and the maximum ripple of the RSSI is 30 mV. The proposed RSSI circuit is fabricated with a personal handy-phone system transceiver. The active area is 0.8 × 0.2 mm^2.**

***Index Terms*—Logarithmic, peak detector, power detector, RSSI, VGA**

I. INTRODUCTION

In wireless communication, received signal strength indicator (RSSI) has a crucial role in detecting received power because, it provides the information necessary to adjust the receiver's gain and helps to select suitable mobile base station. For typical wireless communication applications, RSSI circuits should have a wide range over 60 dB with fast settling time using the received start-up signal [1]. But the wide range RSSI with fast settling time is a difficult problem to achieve at the same time. Also, constant linearity and small ripple of the RSSI for the process and voltage variation are major requirements. Further, it would be useful to have low power consumption without any external component.

Traditional RSSI circuits are generally realized in a logarithmic-linear form to cover several order of signal magnitude using successive-detection architecture. It requires an external large capacitor for a small signal ripple for low pass filtering, so that it makes slow settling time from the receiver power-on signal [2]. Besides, the rectifier and limiter used in conventional RSSI circuit typically have a range about 10 dB. The small logarithmic-linear conversion range needs many rectifiers and limiters to cover several orders of signal magnitude. In addition, the limiter prevents accurate gain control and back-end digital processing after analog-to-digital converter (ADC) [3]. Therefore, the architecture has been used in old fashioned receiver, such as amplitude shift keying demodulator. Recently, with system-on-chip trends, many receivers contain ADCs and digital processing blocks. So, the RSSI value measurement using the backend ADC in RX chain is widely used. But the method also requires automatic gain control time and DC elimination time in the receiver chain before the RSSI measurement. Because it need adjusted input signal level of the backend ADC. Also, the group delay of the RX chain before RSSI calculation is not ignored. Usually, it makes settling time over 100 μs. Therefore, the technique is suitable for the limited application where the relatively long time margin is guaranteed, such as code division multiplexing access (CDMA).

This paper describes a fast RSSI circuit using wide range power detectors, which provide wide range and robustness to process and temperature variation. The power detector circuit is consisted of a wide range logarithmic

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gain amplifier, a peak detector, a comparator and a low pass filter and it does not require any external component.

II. ARCHITECTURE OF RSSI CIRCUIT

The proposed RSSI block diagram is shown in Fig. 1. The RSSI structure is based on a conventional direct conversion receiver. The RSSI value is measured by wide range power detectors at fixed signal points, digitized by single ADC, and processed by small digital processing block for more averaging and compensation. In this architecture, key block is the wide range power detector, in the sense that this block decides the total number of power detector and the resolution of the ADC. When the range is very wide, just one power detector can cover whole RSSI range. But this causes the steep increase of the dynamic range of power detector and the ADC resolution. As a result, the overall area and complexity of RSSI circuit will increase too much. In this design, a power detector which has 36 dB detection ranges is used in 3 points and 6-bit ADC is used, which are traded-off between power consumption and area. Fig. 2 shows how the ADC shares 3 power detectors. The ADC operating 9.6 MHz changes the input port to the outputs of the power detectors by rotating sequentially. The ADC adopts a logarithmic architecture to reduce extra area and power consumption. And small digital processing block provides an extra filtering, temperature compensation, and gain weighting. Our targeted total RSSI range is about 70 dB. By using 3 power detectors, we can obtain the range with overlapping margin for gain mismatch.

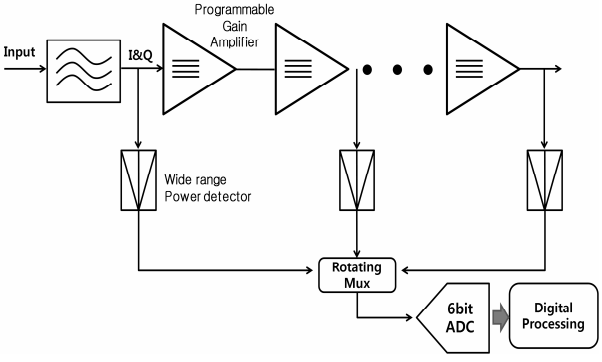


Fig. 1. Block diagram of the proposed RSSI architecture.

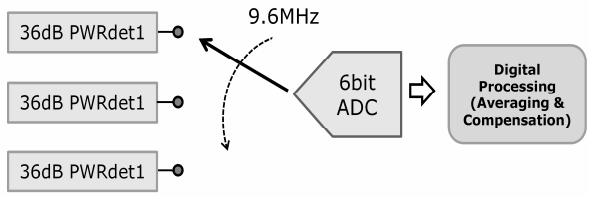


Fig. 2. Shared ADC for 3 power detectors.

III. DESIGN OF RSSI CIRCUIT

1. Wide range power detector structure

Fig. 3 shows architecture of the proposed wide range power detector. It adopts a widely used closed loop structure which consists of a logarithmic amplifier, a peak detector and a comparator. When an input signal comes into the power detector, the signal is amplified in logarithmic scale by a gain control voltage. The amplified signal is converted to a dc level which is proportional to the input magnitude by a peak detector. The peak detector shows a stable output signal without any filtering, using orthogonal characteristics of in-phase and quadrature-phase signals. The dc level, proportional to input power level, is compared with predefined reference voltage and will tracks the reference voltage by feedback loop. Finally, the output of comparator is filtered and affects the gain of logarithmic amplifier, so that control voltage is proportional to input power level. The filtering capacitor decides bandwidth of this closed loop transfer. In this design, 10 pF capacitor is selected to achieve the bandwidth of the closed loop is set to 1 MHz.

2. Logarithmic Gain Amplifier

The logarithmic amplifier is a main block of the power detector, because it decides the total range of power detector and minimum detecting level. In order to cover wide range, a logarithmic characteristic is helpful for RSSI

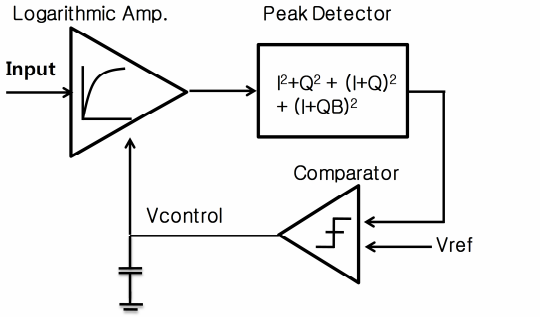
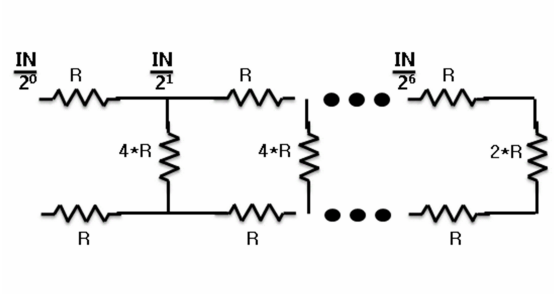


Fig. 3. Structure of the wide range power detector.

operation [4,5]. There are several types of variable gain amplifier (VGA) that have logarithmic transfer characteristics. The most conventional logarithmic amplifier uses a weak inversion region in input transistors to achieve exponential gain [6,7]. So, the input bias level should be set very carefully. And the logarithmic amplifiers adopt open loop type structure using cascode structure for the gain control, but the open-loop structure tends to change easily its gain transfer characteristics and frequency response by the process, voltage and temperature variation. Also, the gain linearity is not always constant. Therefore, the proposed power detector incorporates a closed-loop type VGA instead of open loop, as shown in Fig. 4. First,



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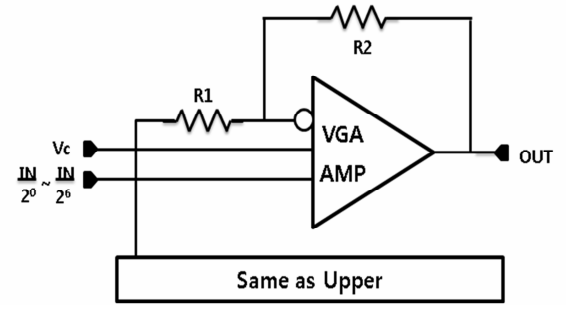

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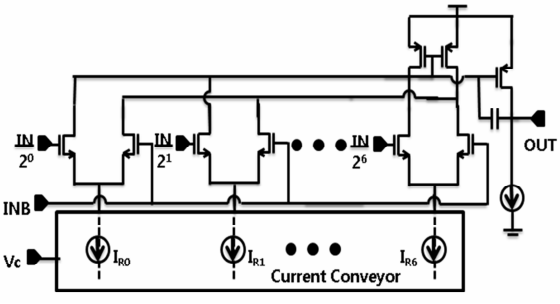


(c)

Fig. 4. Architecture of logarithmic gain amplifier (a) R-2R Resistor ladder, (b) VGA structure, and (c) amplifier core schematic.

in Fig. 4 (a), a R-2R ladder is used to segment the input signal by the voltage level of the logarithmic form. And the divided signals are inputted to the VGA core amplifier adopted pseudo-differential structure, as shown in Fig. 4 (b). The core amplifier used the VGA is shown in Fig. 4 (c). The amplifier uses a well-known two stage amplifier for high gain. A current conveyor that can select input by controlling current sources connected input pairs voltage is used for the gain control in the VGA. The current conveyor operates as follows. When control voltage is high level, the selected input will be the port connected a large input signal level. On the contrary, when the control voltage goes low, the input pair connected a small input level is selected. Therefore, the gain of VGA is decided by input signal selection controlled in the current conveyor, because the feedback configuration is unchanged. The maximum gain of the VGA is achieved when the input signal is applied without any attenuation. When input signal is attenuated at most, the gain of the VGA is minimized. So, the gain range of the VGA is as shown in (1).

$$Gain\ \ Range : (1+\frac{R2}{R1})\times\frac{1}{2^N}\ \sim\ (1+\frac{R2}{R1}) \qquad (1)$$

The input pair of the amplifier is divided into N segments according to input signal level in R-2R resistor ladder. In this design, we select 6 segments of input signals taking area and complexity into consideration. A current conveyor supplies tail currents of the six input pairs. So, when the gain control voltage of VGA comes into current conveyor, one of input pairs is activated strongly, whereas others are turned on slightly, or turned-off. As a result, the input signal adjusted by the control voltage is amplified by

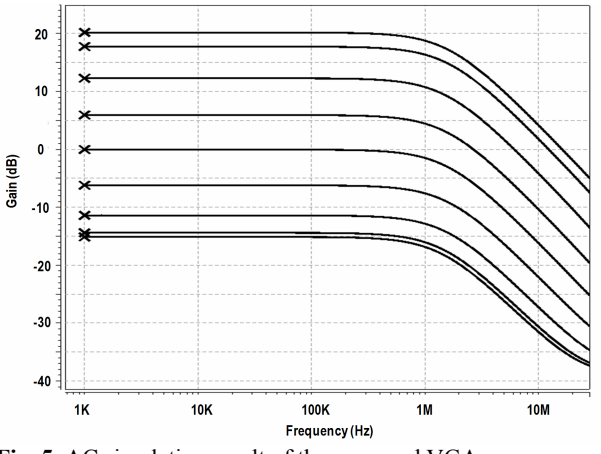


Fig. 5. AC simulation result of the proposed VGA.

a fixed gain. The AC simulation result of the VGA is shown in Fig. 5. It shows that about 36 dB gain range is obtained by increasing the control voltage. By the simulation result, the gain characteristic is almost the same to temperature, process variations.

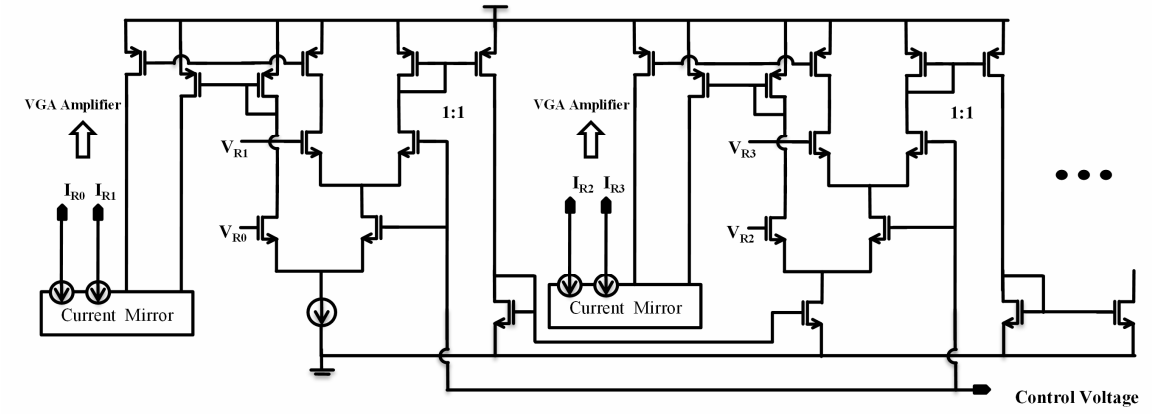
Fig. 6 (a) shows a schematic of the current conveyor that supplies tail currents proportional to the control voltage to input pairs of the VGA. It consists of the number of comparators which are connected various reference levels. The gain control voltage of the VGA is compared with the reference voltages in the comparators. To have wide range detection in low supply voltage, the comparators are implemented using stacking and current mirroring. Under 1.8 V supply voltage, 2 stacking in a row are suitable, considering voltage headroom. And the stacking comparator is cascaded by current mirroring. When the control voltage is increased higher than the low reference voltages (V_{R0}, V_{R1}), the currents in the paths of I_{R0}, I_{R1} will be decreased. However, currents related to high reference voltages (V_{R2}, V_{R3}, V_{R4}) are coming to activate in rows. The ideal current waveform is shown in the Fig. 6 (b). As the control voltage increases, activated current sources are changed sequentially. As a result, very wide range of control voltage can be achieved.

3. Peak detector

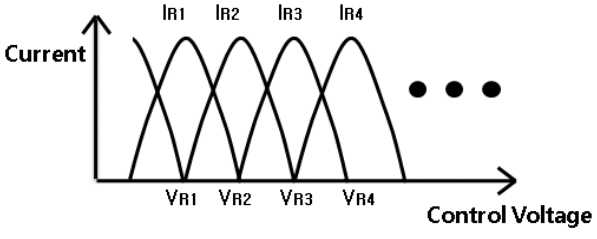
A peak detector in the power detector has a role of converting incoming signal to a stable dc signal proportional to the magnitude of the input signal. The peak detector is designed to have a range about 15 dB. It doesn't have to have wide range by reason that the output of peak detector always goes around the reference voltage in the closed loop of Fig. 3. In this design, a multiplier of gilbert-cell type is used for the peak detector since quadrature signals with orthogonal characteristics can be easily processed to a dc level without any filtering.

$$\begin{aligned} I^2+Q^2 &\Rightarrow A^2COS^2\theta + A^2SIN^2\theta = A^2 \\ (I+Q)^2+(I+QB)^2 &\Rightarrow (ACOS\theta + ASIN\theta)^2 + (ACOS\theta - ASIN\theta)^2 = 2A^2 \end{aligned} \quad (2)$$

Equation (2) shows the peak detection method using the orthogonal characteristics of quadrature signals which is used in this design. Conventional peak detector makes dc value by only using I^2+Q^2 [8]. But, to minimize the output ripple of peak detector with fast settling time, extra multiplier using $(I+Q)^2+(I+QB)^2$ is used in this design for more averaging. Summing the signals is made by simple current



(a)



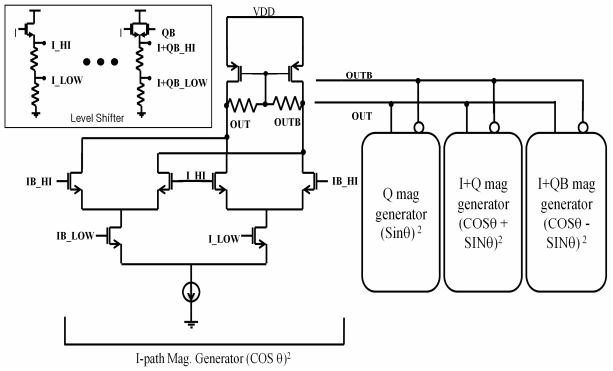
(b)

Fig. 6. The current conveyor : (a) schematic and (b) waveform of output current.

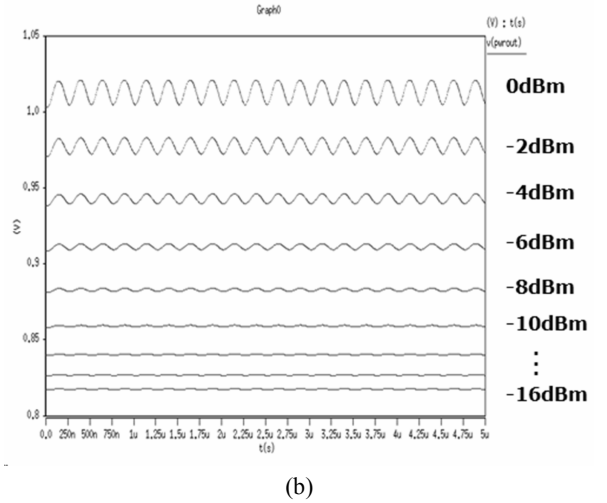
adders. Detailed schematic of peak detector is shown in Fig.7 (a). Fig. 7 (b) shows the transient simulation result according to the varying input power level from -16 dBm to 0 dBm. It shows that stable dc levels proportional to the input power are generated, despite of changing input signal.

4. Post processing

To accommodate output of power detector, a 6-bit ADC is used to sample the outputs of power detectors using rotating analog switches. The output of ADC is passed to a digital signal processing block which is consisted of simple adders [9]. According to the location of power detector, different gain weightings are added at the data. For example, the power detector in front gets the weighting which is a cumulative gain until previous stage. The weighting values can be changed by temperature variation and gain variation. Moving averaging is also added for more stable RSSI value with digital processing. But, the averaging can be increase the settling time of the RSSI. So, the averaging factor is traded-off. For verification, a digital-to-analog converter (DAC) is used to report an analog signal through an external pin.



(a)



(b)

Fig. 7. Peak detector (a) structure, (b) simulation result.

IV. EXPERIMENTAL RESULTS

The proposed RSSI circuit has been fabricated using 0.18-μm one-poly five-metal CMOS technology. The chip photograph is shown in Fig. 8. And the area of the RSSI circuit is 0.8 mm x 0.2 mm including 3 power detectors, ADC, and digital processing block. Actually, in that area, 4 power detectors are drawn, 3 are for the RSSI, the other is for a transmitter which is for transmitting power measuring. The simulated and measured results of the VGA are plotted in Fig. 9. The gain transfer curve is almost same. Fig. 10 shows the measured characteristics of the proposed RSSI circuit. By using a serial-to-parallel interface (SPI), it is possible to find and calibrate the optimum RSSI range of each power detector by controlling suitable weighting value. The range of the signal detection is about 70 dBm, as shown in Fig. 10 (a). The minimum detection

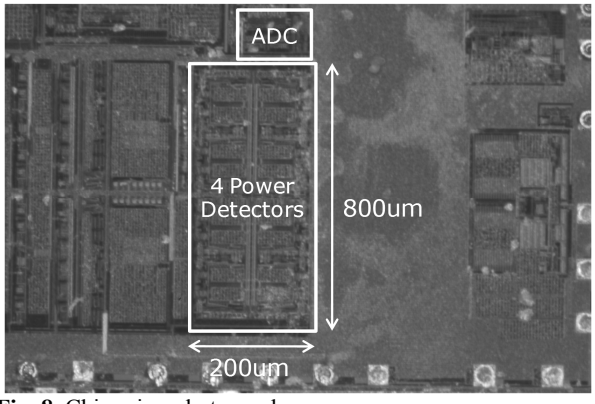


Fig. 8. Chip microphotograph.

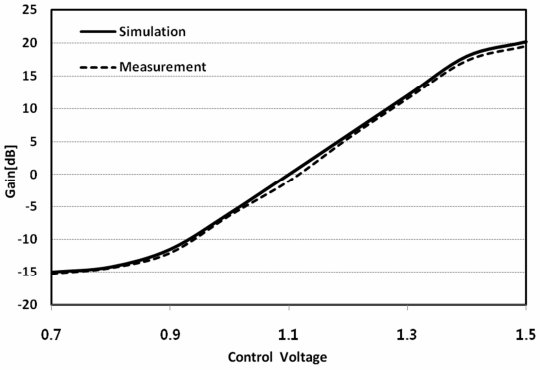
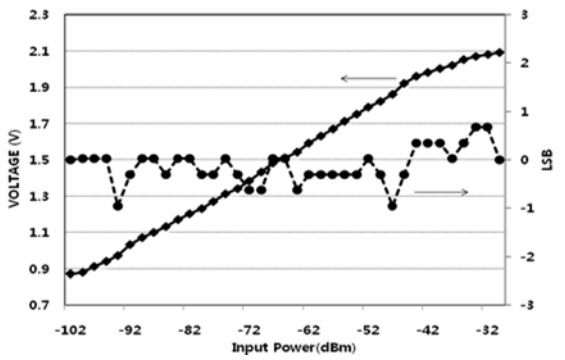
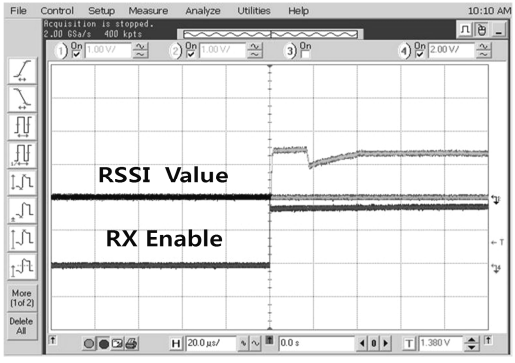


Fig. 9. Characteristic of the proposed VGA.



(a)



(b)

Fig. 10. Measured RSSI : (a) transfer curve, (b) transient response.

value is -102 dBm that is limited by receiver sensitivity, and the maximum is limited to -30 dBm by RF gain stage. The ripple of the RSSI is under 30 mV_{P-P} which is corresponding to 1 LSB. 1 LSB is corresponded to the value from full voltage range by 70 dB. The settling time of the RSSI is about 40-μs from receiver enable signal as shown in Fig. 10 (b). But, the input signal of the RSSI comes after 20 μs because of locking of local oscillator, the effective settling time of the RSSI is 20 μs. The total power consumption of the proposed RSSI is 20 mW including three power detectors, an ADC and a digital logic block.

ACKNOWLEDGMENTS

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