A Transconductor and Tunable $G_m - C$ High-Pass Filter Linearization Technique Using Feedforward G_{m3} Canceling

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***Abstract*—A linearization technique of a transconductor circuit is proposed in this brief. By adopting a two-path feedforward architecture, the G_{m3} component of the transconductor vanishes and a highly linear V-to-I conversion is achieved. This technique consists of self-biased inverters only, and it can be applied to transconductors with differential inputs. It also has an advantage in process scaling and precise bias control is not necessary. A tunable $G_m - C$ high-pass filter for the baseband of a frequency–modulated continuous-wave radar system is implemented using these linearized transconductors. The filter is synthesized with a high-order admittance method. The designed filter is fabricated in a 0.13-μm CMOS process. The filter cutoff frequency can be tuned from 0.15 to 0.75 MHz with a current consumption value of 11–36 mA. An in-band input-referred third-order intercept point of $+19.4$ dBm and a 1-dB compression point of $+5.35$ dBm are measured, demonstrating a highly linear filter operation.**

***Index Terms*—$G_m - C$ filter, linearization, transconductor, tunable high-pass filter.**

I. Introduction

THE demand for highly linear circuits to support various wireless communication standards is increasing. To process in-band signals and prevent such signals from being disturbed by unwanted blockers or interferers, the receiver front end must consist of circuits with high linearity. If the circuits are cascaded, the nonlinearity components of the latter stages become more critical [1]. Therefore, the input-referred third-order intercept point (IIP3) performance of the latter stages plays an important role in the linearity of the overall system. Since the filters for channel selection or rejection are usually located in the last stage of the receiver front end, the design of a high-performance intermediate frequency or baseband filters is necessary.

To enhance linearity, the multiple-gated-transistor (MGTR) method is widely used [2], [3]. This technique uses two or more parallel transistors with different gate widths and gate bias voltages to cancel the third-order derivative g_{m3} of the transistor. The IIP3 value of the transistor improves, where the g_{m3} value is close to zero. However, the MGTR method has drawbacks in that the linearity improvement is achieved by precise bias voltage adjustment. To cancel the g_{m3} component, the gate width and gate bias must be controlled to find the optimum operation point, which means that the MGTR method is sensitive to bias variations.

Linearity improvements can be also achieved using the feedforward method [4], in which two paths are used to actively cancel the nonlinearity. In addition, it requires accurate scaling between the input signals of the main and auxiliary paths to perform exact cancelation. However, the circuits that generate the scaled inputs for both paths are not shown in [4].

A method of attenuation–predistortion in [5] also uses two paths for the linearization. In this architecture, an attenuated input signal is required for the auxiliary path, and a digitally controlled phase shifter is needed to compensate the mismatches and the process–voltage–temperature variations.

An active-RC filter [6] is known for its high linearity. However, the cutoff frequency tuning of the active-RC filter is performed by switching capacitors and/or resistors in the filter, which provide discrete frequency tuning. Another candidate is $G_m - C$ filter [7]. Although it has lower linearity than active-RC filter, it can be continuously tuned by changing the bias current.

In this brief, a linearization technique of the transconductor circuit is proposed. The proposed technique is based on the feedforward method, and it actively cancels the G_{m3} component of the transconductor, which is the main contributor to the nonlinear V-to-I conversion. This technique is explained in Section II. In Section III, a tunable $G_m - C$ high-pass filter design adopting linearized transconductor circuits is presented. Section IV deals with the measurement results of the fabricated filter circuit and Section V concludes this brief.

II. Transconductance Linearization Technique

In MOSFET devices, the drain current I_d can be expressed with Taylor expansions as

$$I_d = g_{m1}V_{gs} + g_{m2}V_{gs}^2 + g_{m3}V_{gs}^3 + \cdots \tag{1}$$

where V_{gs} is the gate-to-source voltage of the device and g_{mn} is the nth-order derivatives of the drain current I_d with V_{gs}. Like a MOSFET device, a transconductor circuit can be modeled

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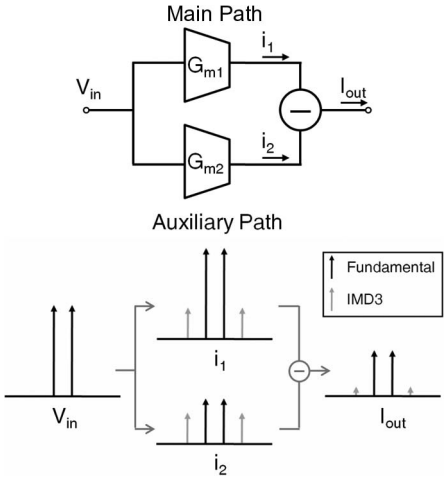

Fig. 1. Block diagram of the proposed transconductor linearization technique.

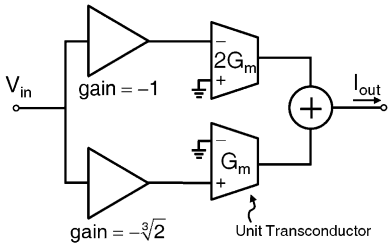

Fig. 2. Block diagram of two-path G_{m3} cancelation using a linear voltage amplifier.

using the same expression. The output current of the circuit consists of a polynomial of the input voltage $V_{\rm in}$ and the transconductance G_m, which becomes

$$I_{\rm out} = G_{m1}V_{\rm in} + G_{m2}V_{\rm in}^2 + G_{m3}V_{\rm in}^3 + \cdots . \tag{2}$$

To make the voltage-to-current conversion a linear operation, the $I_{\rm out}$ term must contain the components of G_{m1} and $V_{\rm in}$ only. Assuming that the even-order coefficients can be eliminated with a differential architecture, the main contributor to nonlinearity is the G_{m3} component. Higher order components over fourth derivatives are neglected in this method. Then, a transconductor circuit can be modeled as

$$I_{\rm out} \approx G_{m1}V_{\rm in} + G_{m3}V_{\rm in}^3. \tag{3}$$

Linearization can be achieved by canceling the G_{m3} component. The proposed transconductor linearization technique consists of two paths, as shown in Fig. 1. Transconductors with different G_m values are located in the main and auxiliary paths. The output currents i_1 and i_2 of each transconductor can be modeled with (3). As the third-order intermodulation distortion (IMD3) components of each path are designed to have the same magnitude, they are subtracted and eliminated in the output current $I_{\rm out}$.

Fig. 2 shows the linearization technique with specific values. In the main path, the input voltage is $V_{\rm in}$, and the transconductance is $2G_m$, which means that the two-unit transconductor circuits are connected in parallel. In the auxiliary path, the input voltage to the transconductor is $(-\sqrt[3]{2}V_{\rm in})$, and the transconductance is G_m (unit transconductor). The negative sign at the amplifier output signifies the opposite polarities at the input

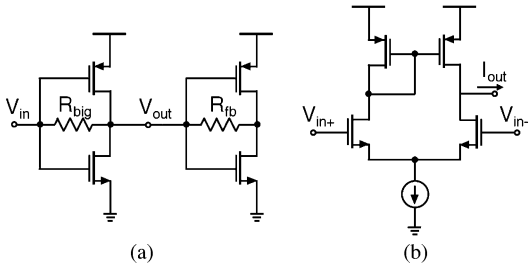

Fig. 3. (a) Schematic of a linear voltage amplifier. (b) Schematic of a unit transconductor circuit.

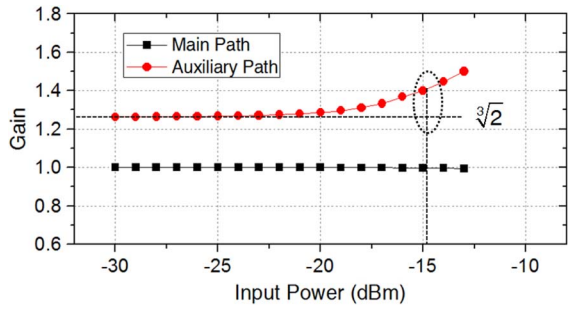

Fig. 4. Simulated gain of the main and auxiliary paths.

and the output. Due to this feedforward auxiliary path, $I_{\rm out}$ is given by

$$\begin{aligned} I_{\rm out} &= i_1 + i_2 \\ &= 2G_{m1}V_{\rm in} + 2G_{m3}V_{\rm in}^3 + \left(-\sqrt[3]{2}G_{m1}V_{\rm in} - 2G_{m3}V_{\rm in}^3\right) \\ &= \left(2 - \sqrt[3]{2}\right) G_{m1}V_{\rm in} \end{aligned} \tag{4}$$

which means that a linear V-to-I conversion is possible. The linear conversion is obtained by increasing the power consumption and reduction of $G_m(2 - \sqrt[3]{2} \approx 0.74)$.

In this linearization method, input voltages of $V_{\rm in}$ and $(-\sqrt[3]{2}V_{\rm in})$ must be applied to each transconductor to perfectly cancel the G_{m3} component. To obtain an input voltage of $(-\sqrt[3]{2}V_{\rm in})$, the linear voltage amplification circuit in Fig. 3(a) is used [8]. In [8], the voltage amplifier consists of a driving inverter and a loading inverter. This self-biased inverter-based circuit can amplify the input voltage linearly.

To reduce the phase mismatch of main and auxiliary paths for perfect cancelation, another linear voltage amplifier, which has gain of (-1), is inserted in the main path. The transconductor circuits with differential inputs are used to create opposite polarities in the two paths.

Fig. 3(b) shows the unit transconductor circuit. A basic differential pair is used for the differential input, and a current mirror load is implemented to obtain a single-ended output current. The transconductance of the circuit can be adjusted by the tail current, which mirrors the current of an external reference current source.

Since the active G_{m3} canceling architecture does not alter the original transconductor circuit, this technique can be easily applied to conventional transconductors with differential inputs. In addition, this linearization technique is independent of the bias variations of the transconductor. As reported in [8], the gain of the linear voltage amplifier is defined by the G_m of the inverters and $R_{\rm fb}$. Therefore, the ratio of the two paths is insensitive

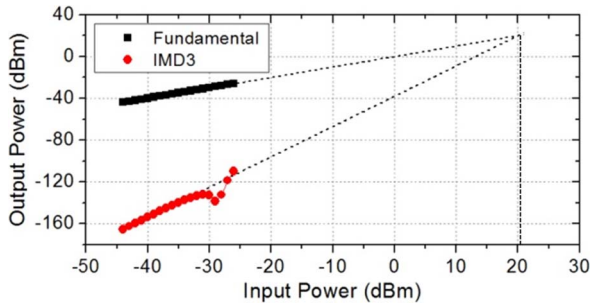

Fig. 5. Simulated IIP3 of the voltage amplifier.

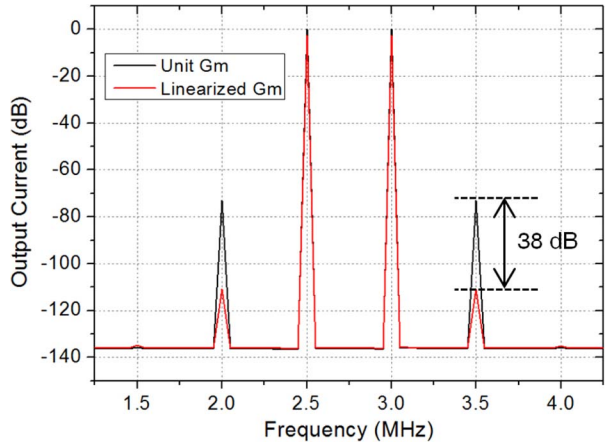

Fig. 6. Simulated difference in the IMD3 current between the unit transconductor and the linearized transconductor.

to the bias voltages, which means that any value of the G_{m3} component can be eliminated, whereas the main and auxiliary paths maintain a voltage amplification ratio of $1:\sqrt[3]{2}$. Fig. 4 shows the simulation result of the voltage amplifiers in the two paths. The ratio of the two paths holds up to the input power of -20 dBm, and the gain error reaches 10% when the input power is -15 dBm. This result demonstrates that G_{m3} cancelation can be performed up to the input power of -15 dBm with small errors.

The linearity of the voltage amplifier is critical for the G_{m3} cancelation. Fig. 5 presents the two-tone linearity simulation result of the voltage amplifier. The IIP3 of $+20.4$ dBm shows highly linear operation of the amplifier.

The G_{m3} cancelation simulation between the unit transconductor and the linearized transconductor is shown in Fig. 6. Equal input voltage signals of 2.5 and 3 MHz are applied to the transconductors, and the output current of each circuit is plotted in decibel scale to verify the proposed technique. The result shows that the IMD3 component of output current at 3.5 MHz is reduced by 38 dB due to the linearization circuit. However, the improvement of IMD3 is achieved by increasing power consumption by the factor of 5 when compared with the unit transconductor, and input-referred noise power increased by the factor of 8.2.

III. Design of Tunable High-Pass Filter

In a frequency-modulated continuous-wave (FMCW) radar system, the distance from the target is proportional to the baseband frequency of the system [9]. A filter is necessary in the receiver baseband of a through-the-wall FMCW radar system to reject the antenna coupling and wall-reflected waves [10], [11]. In a situation in which the target exists beyond the wall, a high-pass filter can attenuate the unwanted wall-reflected waves. The high-pass filter must have a tunable cutoff frequency because the distance from the through-the-wall radar to the wall can vary.

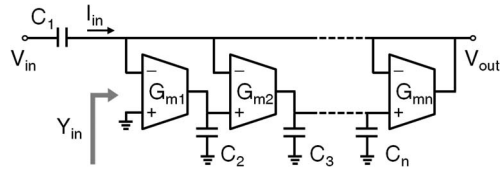

Fig. 7. High-pass filter using high-order admittance element synthesis.

A tunable $G_m - C$ high-pass filter in [12] is designed using the linearized transconductors. This filter of order N can be synthesized using N transconductor circuits and N capacitors.

Fig. 7 shows the Nth-order high-pass filter with high-order admittance element synthesis. The input voltage is divided into C_1 and Y_{in}, making the transfer function from input to output as

$$\begin{aligned} H(s) = \frac{V_{\text{out}}}{V_{\text{in}}} &= \frac{sC_1}{sC_1 + Y_{\text{in}}(s)} \\ &= \left[s^n \Big/ \left(s^n + \frac{G_{mn}}{C_1} s^{n-1} + \frac{G_{m(n-1)}G_{mn}}{C_1 C_n} s^{n-2} \right.\right. \\ &\quad + \frac{G_{m(n-2)}G_{m(n-1)}G_{mn}}{C_1 C_{n-1} C_n} s^{n-3} \\ &\quad \left.\left. + \cdots + \frac{G_{m1}G_{m2},\ldots,G_{mn}}{C_1 C_2,\ldots,C_n} \right) \right]. \end{aligned} \tag{5}$$

The designed high-pass filter has a unit filter order of 2, and these unit filters are cascaded to make higher orders to prevent linearity degradation. The normalized transfer function of the second-order filter with the same G_m values becomes

$$H(s) = \frac{s^2}{s^2 + c_{21}s + c_{22}} \tag{6}$$

where the normalized transfer function coefficients for the Chebyshev filter response are given by $c_{21} = G_m/C_1 = 1.1025$ and $c_{22} = G_m^2/(C_1C_2) = 1.0977$. The poles of the transfer function are located at $-0.5497 \pm 0.8954i$. The capacitor values of the filter are set to a cutoff frequency up to 750 kHz, thus becoming $C_1 = 330$ pF and $C_2 = 82$ pF. These capacitors are externally attached; thus, the filter could be adjusted to another cutoff frequency range. By scaling transconductance, the frequency response of the filter is proportionally scaled, which means that the filter can maintain the Chebyshev filter response at any given cutoff frequency.

The final design of the filter is implemented with differential inputs and outputs (see Fig. 8). To avoid the effect of the load on the frequency response of the filter, a voltage buffer is placed after the filter stage.

The frequency response and the phase of the high-pass filter in Fig. 8 are simulated, and the results are plotted in Fig. 9. The frequency response presents the filter operation at the cutoff frequency of 250 kHz, and the phase simulation shows that the filter is stable.

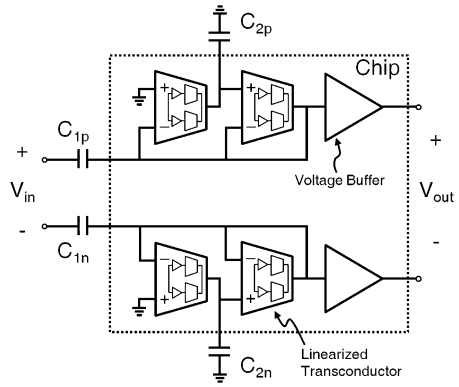

Fig. 8. Block diagram of a second-order unit high-pass filter.

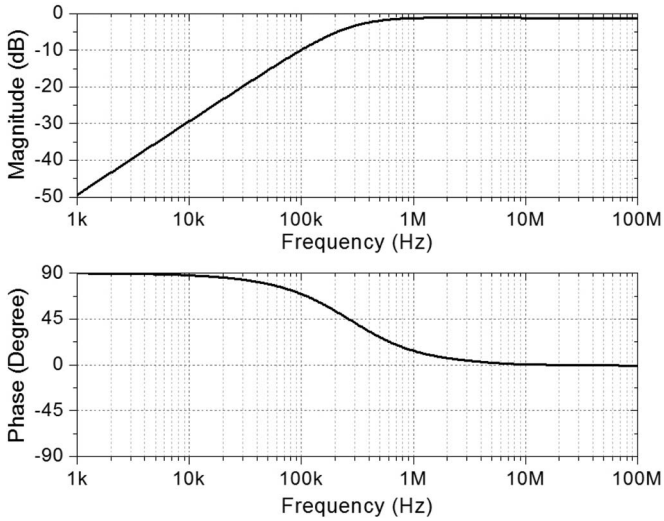

Fig. 9. Frequency response and phase simulation of the high-pass filter in Fig. 8.

IV. Measurement Results

The proposed tunable $G_m - C$ high-pass filter is fabricated using the standard 0.13-μm CMOS process. The whole die size is 700 μm $\times$ 270 μm, and the active area of the filter is 520 μm $\times$ 120 μm without pads. Fig. 10 shows the micrograph of the chip. The power consumption of the fabricated filter is from 13.2 to 43.2 mW when the filter bias current changes from 0 to 0.5 mA. The large power consumption is mainly due to the inverters in the linearization circuit because these self-biased inverters draw a dc current when the VDD is applied. Reducing the size of the inverters in the voltage amplifier will decrease the power consumption, but the linearity of the amplifier may degrade. Moreover, the topology of the linearization technique that uses parallel-connected transconductors also contributes to the large power consumption. If the linearization technique is not applied, the power consumption for the same bias current will be from 2.76 to 7.35 mW.

Fig. 11 shows the tunable frequency response of the filter. By changing the external reference current source, the frequency response can be adjusted continuously. The cutoff frequency of the filter can be tuned from 150 to 750 kHz by the reference current from 0 to 0.5 mA. The filter shows the second-order Chebyshev response, and insertion loss of the filter is 1.1 dB. The cutoff frequency range can be extended with wide tuning of external reference current, but it requires reduction of voltage headroom of the current mirroring circuit in the unit transconductor.

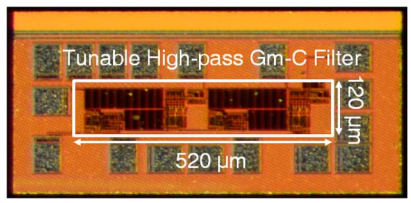

Fig. 10. Chip die micrograph.

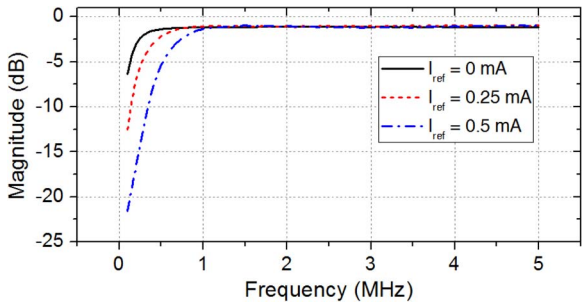

Fig. 11. Frequency response tuning of a high-pass filter.

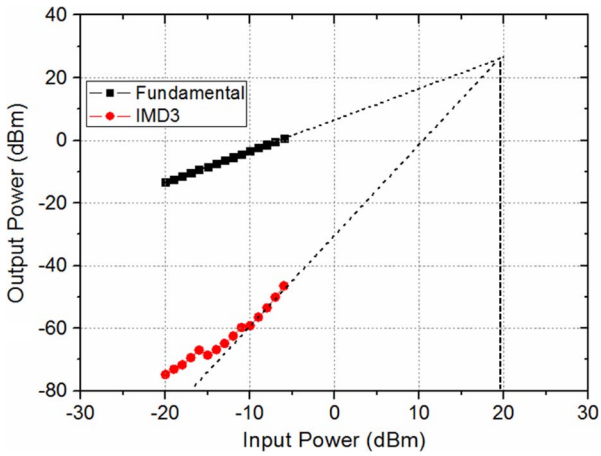

Fig. 12. In-band IIP3 measurement of the high-pass filter.

Fig. 12 presents the in-band IIP3 measurement result of a two-tone test. Input signals of 2.5- and 3-MHz tones are applied for the test, and the measured IIP3 of +19.4 dBm shows the highly linear operation of the filter, as well as proving that the G_{m3} cancelation circuit works.

A single-tone linearity test is performed to measure the 1-dB compression point (P1dB) of the filter. The measured P1dB is at +5.35 dBm, and the gain compression mainly comes from the inverter-based amplifiers in the linearization circuit. The linear operation of the filter leads to achieving the dynamic range of the input power of 77 dB.

The filter performance is summarized and compared with prior research in Table I.

TABLE I
MEASUREMENT RESULTS AND PERFORMANCE COMPARISON

	[3]	[5]	[6]	This Work
Technology (μm)	0.18	0.13	0.13	0.13
Filter Topology	RC-Gm-C low-pass	Gm-C low-pass	Active Gm-RC low-pass	Gm-C high-pass
Linearization Technique	MGTR	Attenuation-Predistortion	-	Feed Forward
Supply Voltage (V)	1.8	1.2	0.55	1.2
Filter Order	3	2	4	2
Cutoff Frequency (MHz)	50-200	200	11.3	0.15-0.75
Tuning Ratio	4	-	-	5
Power Consumption (mW)	23.4	20.8	3.5	13.2-43.2
P1dB (dBm)	-	-	0.5	5.35
IIP3 (dBm)	17.3[a]	14	10	19.4

[a] Extracted value from plot

V. CONCLUSION

A linearization technique of the transconductor circuit that is based on a G_{m3} canceling method has been proposed. Using self-biased inverters and duplicated original transconductors, linearization is easily implemented. It cancels the G_{m3} component of any type of transconductor using the two-path feed-forward method. The inverter-based linearization circuits are insensitive to the bias condition, and the ratio of the two input paths is accurately scaled. To demonstrate the linearization technique, a tunable $G_m - C$ high-pass filter is implemented. The filter is synthesized using a high-order admittance element. The measurement results show a highly linear filter operation, as well as proving that the linearization technique is effective. This technique can be adapted to transconductors with differential inputs, and it has an advantage in process scaling.

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