24 GHz Stacked Power Amplifier With Optimum Inter-stage Matching Using 0.13 μm CMOS Process

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Abstract—**A single-stage 24 GHz triple stacked power amplifier using 0.13 μm CMOS process is demonstrated. To Compare with parallel current combining method, series voltage combining method using a stacked amplifier architecture can realize a large output voltage swing from the top transistor without exceeding the transistor breakdown voltage limitations. However, at high frequencies, parasitic capacitances at the drain of each transistor become significant and it cause the phase difference between output current and voltage swing which degrades the performance of the power amplifier (PA). To solve this problem, the optimum inter-stage matching technique using inductors is introduced. With proposed optimum inter-stage matching method, the power amplifier performs a gain of 12.2 dB and saturated output power of 17.5 dBm with power added efficiency (PAE) of 20.5%. The 3dB output bandwidth is from 20.7-26.8 GHz.**

Keywords-CMOS, power amplifier(PA), stacked transistors.

I. INTRODUCTION

Since the first UWB short range radar system operating at 24 GHz has been developed and introduced in 2005, The automotive radar system market has grown rapidly over the past few years. Automotive radar system increase the drivers safety and convenience by offering the capability to measure the distance and relative speed of objects in front, beside, or behind the car during bad optical visibility or objects hidden in the blind spot during parking or changing lanes [1]. The key factors in driving technology development are low cost and small size in addition to the performance requirement for all weather conditions. As the price of automotive radar is relatively high, CMOS process can be a desirable choice due to its low cost and high integration.

However, comparing with other compound semiconductor process, CMOS process has weak conditions such as low breakdown voltage, high substrate loss, low transconductance and low power density [2]. Especially low breakdown voltage limits the maximum voltage swing across the transistors which makes it difficult to get high gain, high output power in designing high-performance RF PA (power amplifier). In order to overcome the limitations on output power imposed by the constrained voltage swings, some form of impedance transformation and/or power combining must be used.

In this paper, a single-stage 24 GHz triple stacked PA is presented to achieve high output power, operating from a large supply voltage. Connecting transistors in series, the PA can realize a large output swing from the top transistor without exceeding the transistor breakdown voltage limitations. Unlike low-frequency design, however, for a high-frequency design, phase differences of each drain voltage from the stacked transistors cause the degradation of overall power gain and power combining efficiency. This major problem has been reported by many studies [2]-[6]. To solve this problem, an optimum inter-stage matching technique is proposed. Though this technique is still continuing, we have reached certain conclusions.

II. CONCEPT OF THE PROPOSED STACKED POWER AMPLIIFER

A. Basic Operation of Conventional Stacked PA

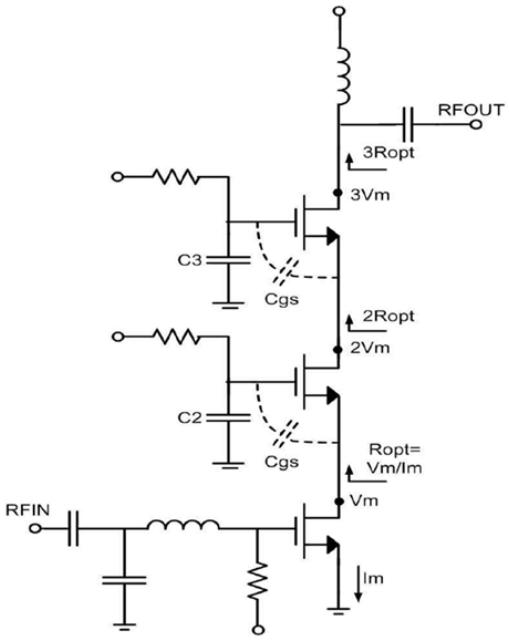

Figure 1. Schematic of conventional triple stacked PA

Conventional triple stacked power amplifier (PA) is shown in Fig. 1. The circuit is composed of a common-source input transistor and two common-gate transistors connected in series so that their output swings are added in phase. Unlike cascode PA, common gates of stacked PA are not RF grounded. Gate capacitances (C2 and C3) are used to allow RF swings at the gates of stacked transistors. The values of gate capacitances (C2 and C3) are determined by the optimum load impedance of the previous transistor so that each transistor can generate the maximum voltage swing and maximum output power. Gate capacitance and gate-to-source capacitance (Cgs) of each stacked transistor form a capacitive voltage divider to produce proper in-phase voltage swing at the gate and drain [2]-[6]. Equations (1)-(2) show how the value of external capacitances (C2 and C3) and device size can be represented.

$$Zin,k \cong \frac{1}{g_m}\left(1+\frac{C_{gs}}{C_k}\right) \qquad (1)$$

$$C_k = \frac{C_{gs,k}}{g_m(k-1)R_{opt,1}-1} \qquad (2)$$

However, at high frequencies, as the effect of parasitic capacitances seen from the drain of each transistor becomes significant, the optimum load impedance of each transistor has reactive value. From (1) above, defining the size of transistor and the value of the external capacitance are not enough conditions to satisfy the required optimum load impedance; it only defines the resistive value of the optimum load impedance. Without considering the reactive values, phase differences across the transistors occur and it cause the fatal degradation of overall power gain and power combining efficiency.

B. Proposed Stacked PA for High Frequency Operation

Fig. 2 shows the schematic of proposed triple stacked power amplifier (PA) for high frequency design. Compare with the conventional stacked PA, additional inductors L1, L2 are used to define the reactive value of each transistor's optimum load impedance. External capacitances and inductors are determined by (3).

$$Yin,k \cong \frac{g_m}{\left(1+\frac{C_{gs}}{C_k}\right)} - j\frac{1}{wL_k} \qquad (3)$$

Optimum inter-stage matching technique by adding inductors can solve the phase differences problem across the transistors and improve the performance of stacked PA in high frequency. However there has a main loss mechanism in proposed stacked PA to look around. Depending on the loss of inductors which are used for optimum inter-stage matching, the efficiency of stacked PA is limited. Fig. 3 shows the power added efficiency (PAE) versus the Q value of inductors. Low loss, high Q value of inductors can generate high performance stacked PA.

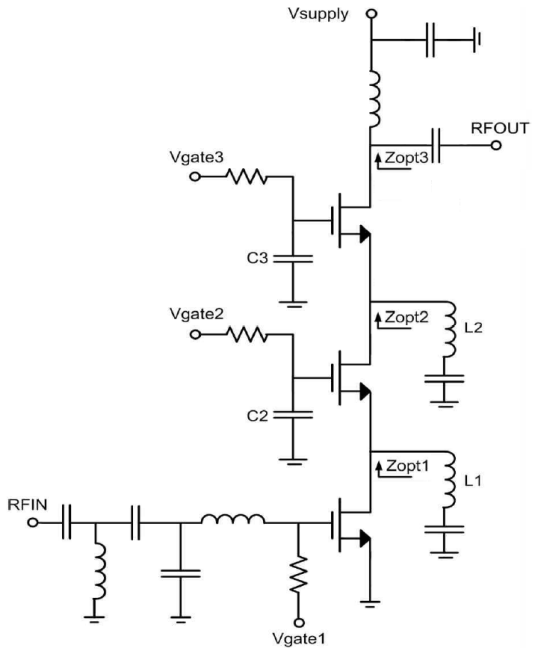

Figure 2. Schematic of proposed triple-stacked PA for high frequency

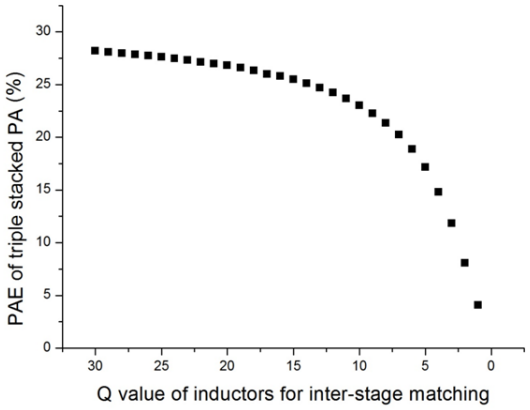

Figure 3. Power added efficiency of a triple stacked power amplifier with the decreasing Q value of inductors.

III. DESIGN OF TRIPLE STACKED CMOS POWER AMPLIFIER

To demonstrate the concepts of the proposed triple stacked power amplifier (PA) design, the standard UMC 130 nm CMOS process is used. The optimum load impedance, optimum load admittance and output power of the transistor are listed in Table1 with respect to the order of stacked transistors. Values are found by using a load-pull simulation. To implement the optimum load impedance, (3) is used for determine the values of external capacitances and inductors. In the final design, the values are slightly modified due to the parasitic effects of interconnection lines during layout.

To reduce the early compression problem at the bottom transistor, total gate width 160 μm is used for common-source transistor and 320 μm is used for each common gate transistor.

TABLE I. OUPUT POWER, OPTIMUM LOAD IMPEDANCE AND ADMITTANCE VERSUS ORDER OF TRANSISTORS

Order of Transistors	Optimum load		Output power (dBm)
	impedance	Admittance	
1	13 + j 7.2	0.059 - j 0.032	14.15
2	24.8 + j 12.5	0.032 - j 0.016	18
3	44.7 + j 14	0.020 - j 0.006	19.50

This PA consumes 168.5 mW of quiescent dc power. Simple input matching network is presented due to its small size of common-source transistor. Output matching network is implemented in low Q region, due to its high output load impedance value, which has the advantage of low loss in output transformation and wide bandwidth. Fig. 4 presents simulated S-parameters of PA. Fig. 5 shows the simulated results of output power, power gain and PAE as a function of input power. The saturated output power is 17.5 dBm with peak PAE of 20.5%. Fig. 6 shows the saturated output power versus frequency. The simulated 3dB power bandwidth is from 20.7 to 26.8 GHz, which corresponds to 25.4% fractional bandwidth. This wide bandwidth covers the requirements of both FMCW car radar system and UWB car radar system operating at 24 GHz.

IV. CONCLUSION

A 24 GHz single-stage triple stacked power amplifier is presented using 0.13 μm CMOS process. To reduce the phase misaligned problems of each transistor which cause the fatal degradation of overall power gain and power combining efficiency, Optimum inter-stage matching technique using inductors is introduced. With proposed optimum inter-stage matching technique, power amplifier performs a gain of 12.2 dB and saturated output power of 17.5 dBm with power added efficiency (PAE) of 20.5%. The 3dB output bandwidth is from 20.7 to 26.8 GHz.

ACKNOWLEDGMENT

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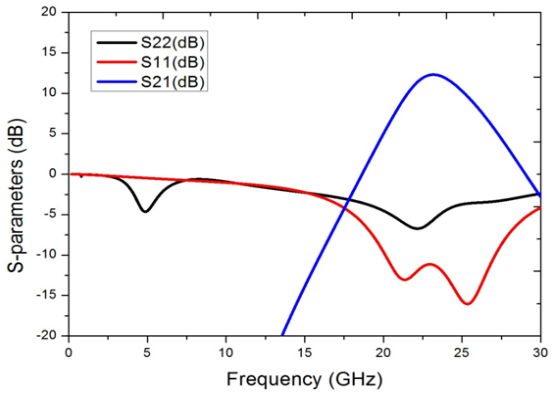

Figure 4. Simulated S-parameters of triple stacked PA

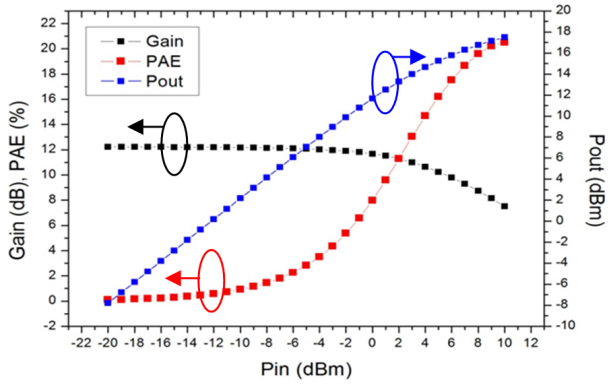

Figure 5. Simulated output power (Pout), power gain, and PAE versus input power

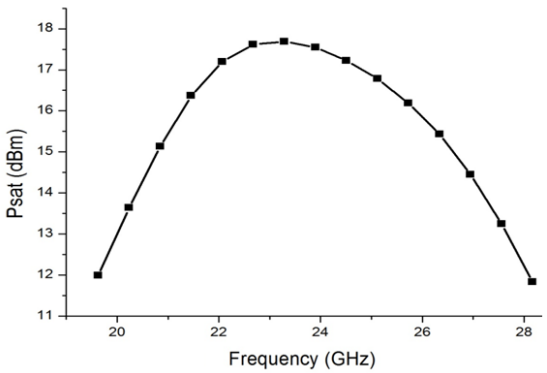

Figure 6. Simulated saturated ouput power (Psat) as a function of frequency

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