Q-band VCO and Injection-locked Buffer for 77-GHz Automotive Radar System in 0.13-μm CMOS

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Abstract —**This paper includes Q-band VCO and high output power injection-locked buffer for 77-GHz FMCW radar system in 0.13-μm CMOS process. The center frequency of the proposed VCO is 34.75-GHz with 1.6% tuning range. The measured phase noise performance shows -102.43 dBc/Hz at 1-MHz offset frequency. The measured maximum single output power is 5.2 dBm and the ideal differential output power is expected to be 8.2 dBm, owing to the injection-locked buffer with a high driving capability. The fabricated chip size is 0.51 × 0.13 mm^2. The power consumption of the VCO core and the injection-locked buffer are 10.8 mW and 50.4 mW from a 1.2 V supply, respectively.**

Key words: Q-band VCO, Injection-locked buffer, FMCW, Automotive radar, CMOS

I. INTRODUCTION

In millimeter-wave automotive radar systems, compound semiconductors have been widely used due to high f_T and breakdown voltage [1], [2]. However, the compound semi-conductor has limitations of its higher cost and lower integration property than CMOS technology when applying to 77-GHz radar system. As performance of CMOS device has been recently improved, CMOS technology has been applied to 77-GHz automotive radar systems [3], [4]. Radar systems can be classified largely into two categories according to principle of wave transmission. One is pulse radar and the other is continuous-wave radar. For pulse radar, it requires high peak-to-average power ratio (PAPR) and wideband operation to generate output short pulse in time-domain, so that CMOS process is difficult to be applied in millimeter-wave pulse radar system because of relatively low supply voltage of CMOS devices. Thus, frequency modulated continuous-wave (FMCW) radar can be a proper candidate for 77-GHz automotive radar system in CMOS process. In the FMCW, one of challenging issues is to generate 77-GHz signal. One way to generate 77-GHz signal is designing 77-GHz oscillator directly and the other way is designing 77/N-GHz oscillator and multiplying N with frequency multiplier. Fig. 1 shows a concept of a 77-GHz FMCW radar transmitter with a 38.5-GHz VCO and a frequency multiplier [5]. In this paper, we present Q-band VCO and high output power injection-locked buffer which can serves as DA. Section II explains circuit description of the proposed VCO and the injection-locked buffer. In Section III, measurement results are presented and conclusions will follow up in Section IV.

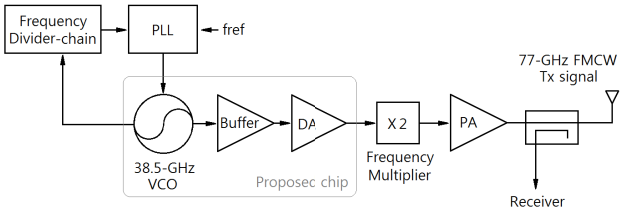

Figure 1. A concept of 77-GHz FMCW radar transmitter.

II. CIRCUIT DESCRIPTION

In this section, the proposed VCO and the injection-locked buffer is described. In general, additional driver amplifier (DA) should be placed between VCO and frequency multiplier, since common VCO buffer cannot generate sufficient power to operate the frequency multiplier well. As the proposed high-power injection-locked buffer can also operates as DA, two blocks, a buffer and a DA, in Fig. 1 can be merged.

A. VCO

The designed Q-band VCO core is shown in Fig. 2(a). It consists of a NMOS cross-coupled pair which provides negative resistance, a PMOS current source and a LC parallel resonator. A dc block capacitor next to the VCO and gate dc bias network of the buffer are not required due to DC voltage drop about 0.3 V from the PMOS current source. Phase noise performance of the designed VCO can be improved, owing to the low flicker-noise characteristics of the PMOS current source and a shunt capacitor which works as a high frequency noise filter at the drain of the current source [6].

B. Injection-locked Buffer

The injection-locking technique means that the oscillator output frequency is locked into the injected periodic continuous signal frequency [7]. Fig. 2(b) shows the designed buffer with injection-locking technique. It has small transistors (M1, M2) to inject signal, a large sized cross-coupled pair to generate high output power, a current source and an inductor. Frequency locking condition and locking range is shown as (1), (2).

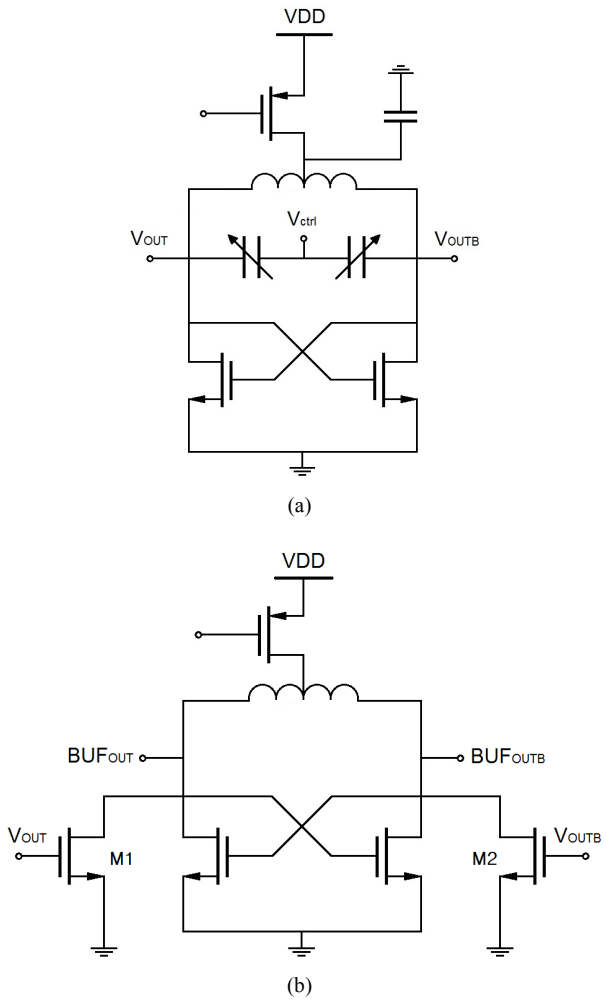

Figure 3. (a) VCO schematic. (b) Injection-locking buffer schematic.

$$|\omega_{inj} - \omega_0| < \Delta\omega_{lock} \tag{1}$$

$$\Delta\omega_{lock} = \frac{\omega_0}{2Q}\frac{A_{inj}}{A} \tag{2}$$

ω_{inj} and ω_0 are the frequency of the injected signal and the frequency of the oscillator, respectively. And $\Delta\omega_{lock}$ is the locking range. In case of the proposed circuit, the injected signal is the VCO output signal and the oscillator is the buffer which oscillates in the steady-state. The injection-locked buffer output frequency is locked into VCO output signal frequency through M1, M2 when (1) is satisfied [8]. Therefore the buffer inductor value should be decided to resonate with capacitance of the cross-coupled pair in the vicinity of the VCO oscillation frequency in order to fulfill the locking condition, (1). In (2), the locking range can be written with ω_0, Q of LC resonator and the amplitude of the injected signal and the oscillator. The signal injection transistors, M1, M2, can prevent high output power of the buffer from leaking into the VCO core owing to its small size. It also operates as the DA, however, since it provides high output power due to relatively large sized cross-

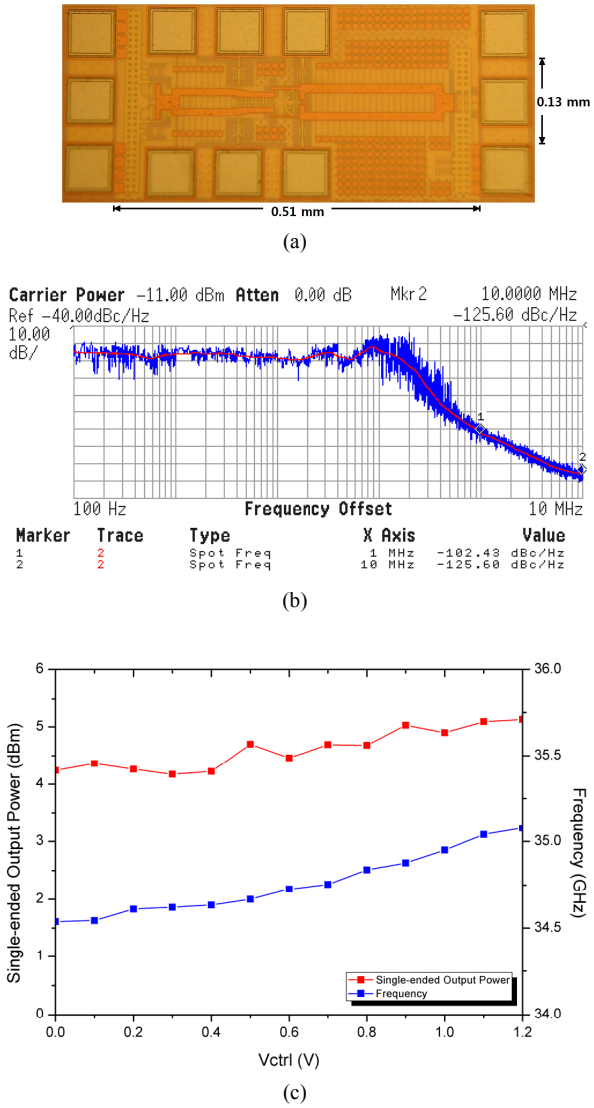

Figure 2. (a) Chip micro-photograph. (b) Phase noise. (c) Single-ended output power and output frequency vs. control voltage.

coupled pair. In the steady-state, the injection-locked buffer oscillates itself, so the buffer output voltage amplitude can be derived by (3) in case of large signal operation.

$$V_{out} = \frac{2I_{bias}R_e}{\pi} \tag{3}$$

In (3), I_{bias} is bias current and R_e is substantive resistance of the buffer which is parallel calculation between load resistance and tank resistance. It shows that the output voltage amplitude is decided by bias current and R_e when the buffer oscillates [9]. Therefore, this buffer can generate high voltage amplitude with large bias current. In conclusion, the injection-locked buffer is the proper solution of merging a buffer and a driver amplifier into one circuit block.

III. MEASUREMENT RESULTS

Fig. 3(a) shows a micro-photograph of the fabricated Q-band VCO and injection-locked buffer in 0.13-μm CMOS. The

TABLE I. THE MEASURED PERFORMANCE COMPARISON

Ref.	Freq (GHz)	Tuning range (GHz)	Pout (dBm)	DC power (mW)		Phase Noise @ 1-MHz	Process	FOM
[10]	37.8	2.2	-19.2	34.7		-90.9	0.18-µm CMOS	-167
[11]	49	0.8	-11	45		-101	0.18-µm CMOS	-178.3
[12]	31.8	2	-	140		-97	0.25-µm SiGe BiCMOS	-165.5
[13]	24	1.7	-	11		-120*	0.13-µm CMOS	-177
This work	34.75	0.6	5.2 (Single)	10.8 (Core)	50.4 (Buffer)	-102.5 -125.6*	0.13-µm CMOS	-186

*Phase noise at 10-MHz

circuit size is 0.066 mm^2, excluding test pads. Measured phase noise performance is -102.43 dBc/Hz at 1-MHz offset frequency and -125.60 dBc/Hz at 10-MHz offset frequency [Fig. 3(b)]. Fig. 3(c) shows the output frequency and the single-ended output power per control voltage. Tuning range is from 34.5-GHz to 35.1-GHz. This is enough to generate 77-GHz FMCW signal because the tuning range is doubled via frequency multiplier. The maximum measured single-ended output power with 50 Ω on-wafer probe is 5.2 dBm when V_{ctrl} is 1.2 V. If the output differential signal has no phase mismatch, the ideal differential output power can be 8.2 dBm. Power consumption of the VCO core is 10.8 mW and the buffer is 50.4 mW from a 1.2 V supply. The figure of merit (FOM) of the VCO is -186 dBc/Hz. The FOM is defined as

$$FOM = L\{\Delta f\} + 10\log\left[\left(\frac{\Delta f}{f_{osc}}\right)^2 \cdot P_{dc}\right] \quad (4)$$

$L\{\Delta f\}$ is the phase noise at Δf offset from f_{osc} and P_{dc} is the dc power consumption (mW). Table 1 shows published Q-band and K-band VCO performances. The results of the proposed circuit seems competitive that it has decent phase noise performance, good FOM and high output power.

IV. CONCLUSIONS

In this paper, the Q-band VCO and the high output power injection-locked buffer for 77-GHz automotive FMCW radar system in 0.13-µm CMOS process. It has decent phase noise characteristics of -102.43 dBc/Hz at 1-MHz offset frequency and the single-ended Pout is around 5 dBm. The tuning range is approximately 600-MHz. Its center frequency is 34.75-GHz which is shifted down about 10% from target frequency. The reason seems to be inaccurate device modeling around the target frequency and parasitic elements which occurs from layout.

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