# An Inductorless CMOS 0.1-1GHz Automatic Gain Control Circuit

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*Abstract*— **This paper presents an inductorless 0.1-1GHz automatic gain control (AGC) circuit comprised of a variable gain amplifier (VGA), power detector (PD), and comparator. The VGA has a gain control range of -28~23 dB with a 1GHz 3-dB gain bandwidth using a cascode amplifier with negative capacitance. The PD shows an input power range of -30~-20 dBm using an improved unbalanced source coupled pair, which incorporates an output differential amplifier and sink current steering. The AGC circuit produces constant output power for an input power range of -48dBm~-8dBm over 0.1~1GHz without an inductor. The overall current consumption is 7.7mA under 1.5V supply. The prototype is fabricated with a 0.18-μm standard CMOS technology.**

## I. INTRODUCTION

Automatic gain control (AGC) circuit is an indispensable building block in many systems where the amplitude of the incoming signal varies over a wide dynamic range, such as Sub-GHz UWB systems or digital multimedia broadcasting (DMB) systems [1], [2]. The AGC circuit provides constant output power and relieves the burden of the input dynamic range at the next stage. The bandwidth and input dynamic range of the AGC circuit are important as the need for wireless high-speed data communication increases.

VGA and PD are key building blocks in the AGC circuit because they determine input dynamic range, settling time, linearity, and bandwidth of the AGC circuit. There are many approaches in the design of VGA to realize the dB-linear gain characteristic to Vcnt, which enables a fast and constant settling time for the AGC circuit [3]–[5], and the wideband characteristic, which enables the wideband AGC operation [6],
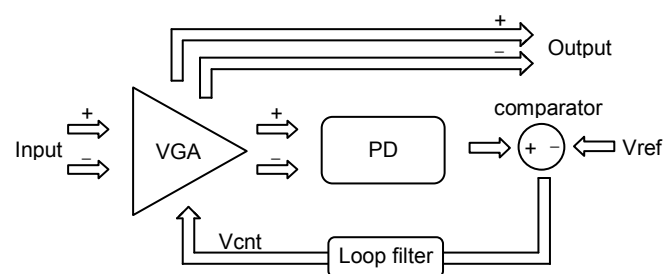
[7]. However, conventional VGAs have limits in wideband realization because they use parallel resonance, which has the frequency selective characteristic. In the design of PD, the use of Schottky diode with a sharp turn-on characteristic is a widely known technique for accurate, low-power detection. Unfortunately, a reliable Schottky diode is difficult to be implemented in a standard CMOS process due to unspecified modelling of Schottky contacts [8]. The unbalanced source coupled pair is a good alternative to the Schottky diode because it is easy to implement in the standard CMOS process [9]. However, sensitivity improvement continues to be a problem.

In this paper, we present new design techniques of VGA and PD to overcome the current problems and realize an AGC circuit with wide bandwidth and good sensitivity. First, we propose wideband negative capacitance to realize wideband VGA. Second, we propose sink current steering to improve the sensitivity of PD. In the following sections, these techniques are explained and verified through simulation and measurement results.

## II. DESIGN OF AGC CIRCUIT

Fig. 1 shows the block diagram of the AGC circuit. When the input signal is applied, the VGA amplifies it by the initial gain. Next, the PD makes the output voltage proportional to the input power and the comparator compares the reference
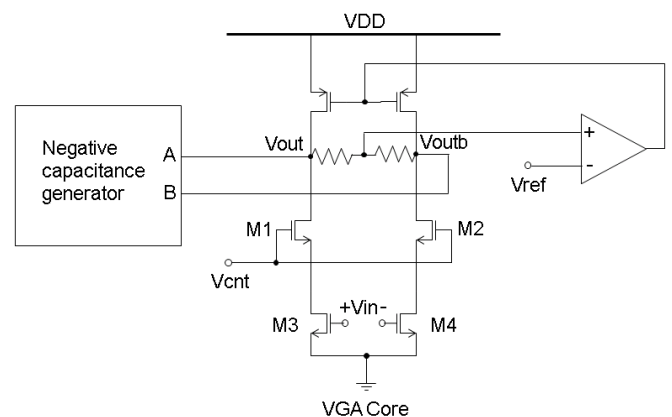


Fig. 1     Block diagram of the automatic gain control circuit



Fig. 2     Schematic of the proposed variable gain amplifier circuit

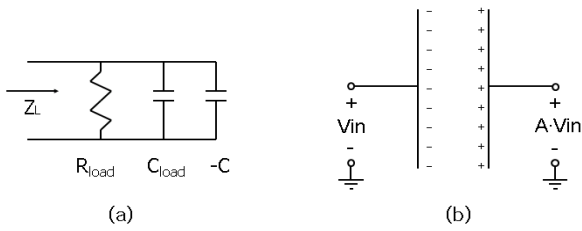October 2008, Amsterdam, The Netherlands

Fig. 3    (a) VGA output load (b) reverse charge accumulation
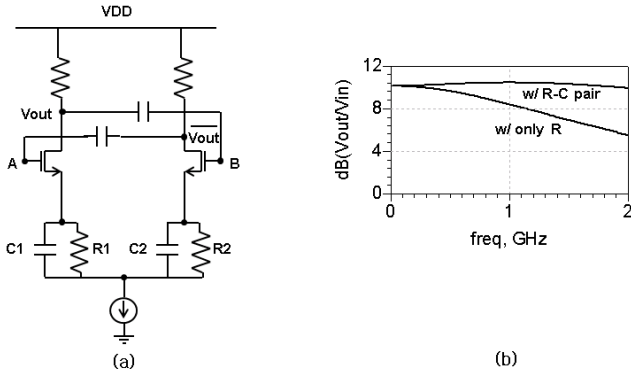


Fig. 4    (a) Schematic of the negative capacitance generator (b) the simulated frequency response of the negative capacitance generator
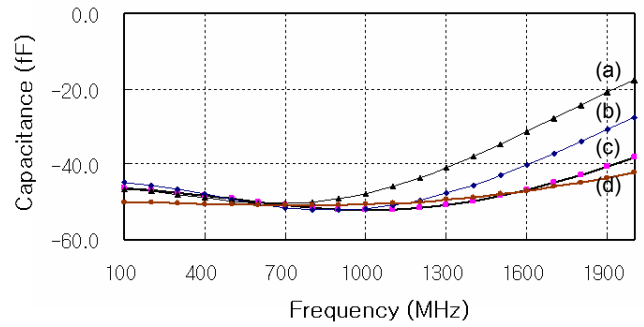


Fig. 5    Simulated negative capacitance with four cross-coupling capacitors. (a) 200fF (5.5dB gain), (b) 160fF (7dB gain), (c) 120fF (10dB gain), (d) 80fF (12dB gain)

voltage (Vref) with the output voltage of the PD. If Vref is higher, the comparator raises the control voltage (Vcnt) of the VGA. Otherwise, the comparator lowers it. As a result, the Vcnt gradually converges to a certain equilibrium point and so does the output power.

### A. Variable Gain Amplifier (VGA)

One of the important requirements of a VGA is a dB-linear gain characteristic to Vcnt, because it enables a fast and constant settling time for the AGC circuit. The cascode structure employed in the VGA realizes it with the specified operation mode of FETs. Common source amplifiers (M3, M4) operate in linear mode, and common gate amplifiers (M1, M2) operate in saturation mode to achieve it [3].

The realization of wide bandwidth is also an important requirement of VGA in wideband applications and it is a focus of the proposed design. There are several techniques to increase the bandwidth of the VGA [6], [7]. These techniques increase the bandwidth by realizing effective inductance, and diminish the effect of output capacitance via parallel resonance. However, it is difficult to realize wideband flat gain with parallel resonance because parallel resonance cannot be effective over a wide frequency range. Thus, the proposed VGA uses negative capacitance instead of effective inductance to increase the bandwidth. The negative capacitance is connected in parallel to the output capacitance, as shown in Fig. 3(a). This method eliminates the effect of output capacitance over a wide frequency range if the negative capacitance is realized over a wide frequency range.

The negative capacitance can be easily realized by the reverse charge accumulation of the cross-coupling capacitor at the differential amplifier, as shown in Fig. 3(b). However, it is

difficult to realize wideband negative capacitance because it is difficult to realize wideband flat gain for the simple differential amplifier. The intrinsic capacitance of the FET and the cross-coupling capacitors increase the output capacitance of the differential amplifier and decrease high frequency gain. Thus, we need a special technique to realize a wideband flat gain up to 1GHz.

The differential amplifier in the proposed VGA uses parallel R-C pairs (R1-C1, R2-C2 in Fig. 4(a)) to realize wideband flat gain. This is possible because there is sufficient voltage headroom, which does not exist in the VGA core because of the cascode structure. These R-C pairs operate mainly as resistors at low frequencies, and mainly as capacitors at high frequencies. They decrease gain at low frequencies by source degeneration of R. The gain at high frequencies remains, however, because the C acts as a short circuit. As a result, the wideband flat gain is achieved as shown in Fig. 4(b).

$$C_{eff} = \frac{Q_{eff}}{V_{in}} = \frac{(1 - A_{DA}) \cdot V_{in} \cdot C_{CC}}{V_{in}} = (1 - A_{DA}) \cdot C_{CC} \quad (1)$$

In order to realize wideband negative capacitance, the selection of $C_{CC}$ (cross-coupling capacitance) and $A_{DA}$ (differential amplifier gain) is important because they affect the gain flatness and power consumption of the differential amplifier. The smaller choice is better for both of these two values. A smaller value of $C_{CC}$ helps to maintain the wideband flat gain of the differential amplifier, so that negative capacitance is constant over a wide frequency range. A smaller value of $A_{DA}$ helps to reduce power consumption. However, these two values should be determined considering required $C_{eff}$ as shown in eq. (1). Thus, the choice should be made by considering the trade-off between $C_{CC}$ and $A_{DA}$.

Fig. 5 shows that 120fF with 10dB gain is the best choice for flat negative capacitance over a wide frequency spectrum in consideration of gain flatness and current consumption. Thus, the proposed VGA uses the differential amplifier with a 120fF cross-coupling capacitor and 10dB gain as a negative capacitance generator. Fig. 5(c) shows the simulated output capacitance of the negative capacitance generator with 120fF cross-coupling capacitors and 10dB gain. It shows flat -50fF output capacitance for the 0.1~1GHz frequency range. The
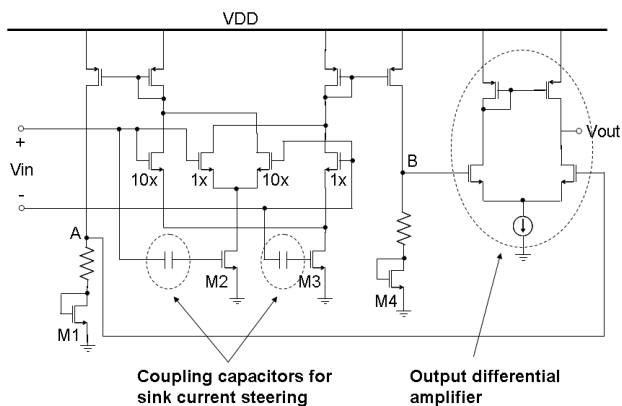
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Fig. 6    Schematic of the proposed power detector circuit.



Fig. 7    Microphotograph of the fabricated AGC circuit



Fig. 8    Measured Freq-Gain curve of VGA for various Vcnt.

resulting wideband negative capacitance reduces the output capacitance of the VGA for the 0.1~1GHz frequency range, and realizes wideband VGA for 0.1~1GHz.

### B. Power Detector (PD)

To be successfully integrated into an AGC circuit, a PD should have a wide bandwidth, high input sensitivity, and a clear output voltage difference for the input power difference. Fortunately, wide bandwidth up to 1GHz is easily obtainable for the CMOS unbalanced source coupled pair because the FET made by CMOS technology has a constant $g_m$ up to 1GHz, which determines the current steering rate.

However, the input sensitivity of a conventional CMOS PD is not good enough to make a clear output voltage difference for incoming RF signals at the PD input without the help of additional internal gain blocks in front of the PD [9]. These gain blocks should be avoided in RF AGC circuits to reduce the risk of oscillation. Thus, the PD in this paper incorporates an output differential amplifier and the proposed sink current steering to improve input sensitivity without the help of additional internal gain blocks in front of the PD.

First, the output differential amplifier improves the sensitivity of the PD. As the input power increases, the voltage levels at nodes A and B move in opposite directions. Thus, sensitivity is improved by connecting the outputs of these two nodes differentially to the inputs of the additional differential amplifier. Second, the proposed sink current steering also improves the sensitivity of the PD. It is realized by using additional input connections that connect differentially to each gate of M2 and M3, as shown in Fig. 6. When the magnitude of the input signal is high, the input connections to M2 and M3 cause more current to steer toward M4 and less current to steer toward M1 regardless of the polarity of input signal. Accordingly, the output differential amplifier and sink current steering improve the sensitivity of the PD.

### C. Automatic Gain Control (AGC) circuit

The VGA and PD determine most of the characteristics of the AGC circuit. However, the loop filter (shown in Fig. 1) determines the loop characteristic, and remains a design issue
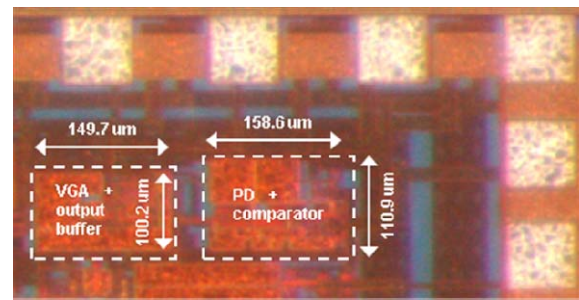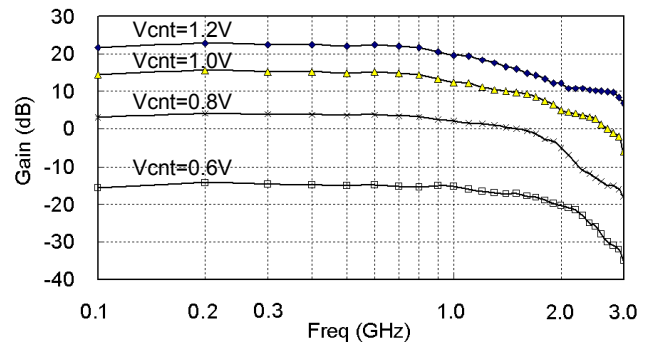
in the AGC circuit. The loop filter is designed as a low pass filter through the tradeoff between fast settling time and stable power convergence. The higher cutoff frequency of the loop filter enables a faster settling time but yields a less stable power convergence. The lower cutoff frequency of the loop filter enables more stable power convergence but yields a slower settling time.

The loop filter in the proposed design is implemented as a simple parallel capacitor of 2nF. This parallel capacitor acts as a low pass filter to yield a settling time of 10μs and stable power convergence.

### III. MEASUREMENT RESULT

The proposed AGC circuit is fabricated using 0.18-μm standard CMOS technology. Fig. 7 shows a microphotograph of the chip. The active area is 150μm x 100μm for a VGA with an output buffer, and 159μm x 111μm for a PD with a comparator. All of these AGC components are tested under 1.5V VDD. The VGA consumes 5.5mA; the PD consumes 1.9mA; and the comparator consumes 0.3mA.

### A. Variable Gain Amplifier (VGA)

Fig. 8 shows the frequency response of the VGA at different control voltages. It shows that the 3-dB bandwidth of the VGA is 1GHz for maximum gain. Fig. 9 shows the gain and input P1-dB curves as the control voltage varies at 500MHz. It shows a quasi dB-linear gain characteristic to Vcnt with a gain control range of -28~23dB and input P1-dB range of -33~-6dBm.

### B. Power Detector (PD)

Fig. 10 shows the Output voltage (Vout) curve as the input
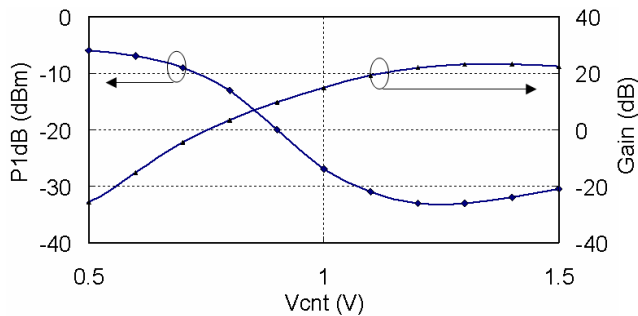
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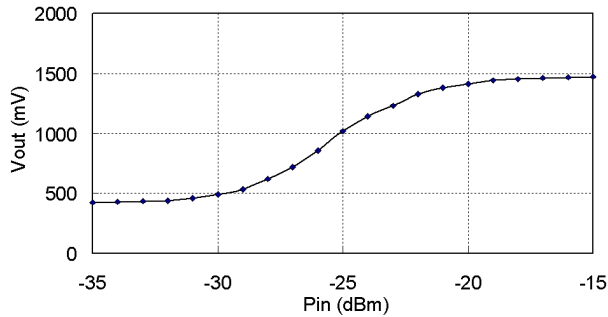Fig. 9    Measured Vcnt-P1 dB/Gain curve of VGA at 500 MHz.



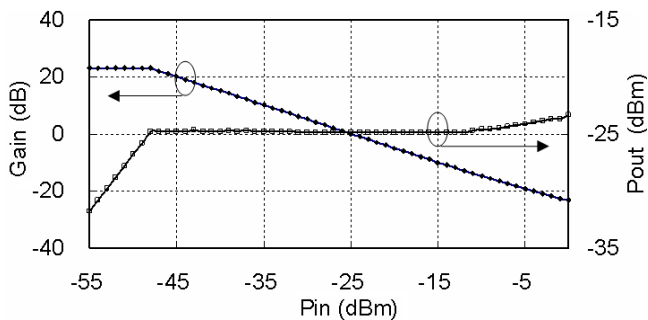Fig. 10    Measured Pin-Vout curve of PD at 500 MHz.



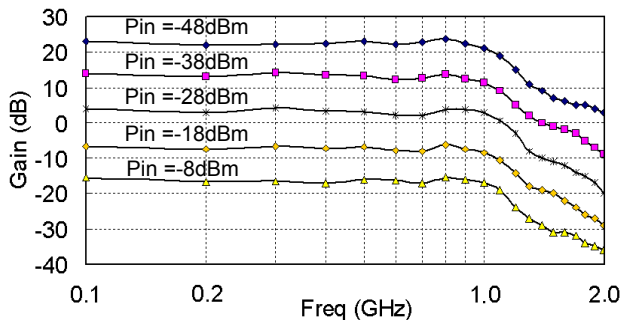Fig. 11    Measured Pin-Gain/Pout curve of AGC circuit at 500 MHz.



Fig. 12    Measured Freq-Gain curve of AGC circuit for various Pin.

power (Pin) varies at 500MHz. It shows a -30~-20dBm input power range for the PD. The frequency-Vout graph for the PD is omitted, but Fig. 12 shows evidence that the Pin difference for the same Vout is within ±2dBm over 0.1~1GHz.

### C. Automatic Gain Control (AGC) circuit

Fig. 11 shows the gain and output power (Pout) as the Pin varies at 500MHz. It shows that the AGC circuit has a -48~-

8dBm input dynamic range at 500MHz within a ±0.5dBm power convergence error. Fig. 12 shows the Pout curve as the frequency varies for various values of Pin. The operating frequency range of the AGC circuit is 0.1~1GHz within a ±2dBm power convergence error for a -48~-8dBm input dynamic range.

## IV. CONCLUSION

An inductorless 0.1~1GHz AGC circuit is fabricated using 0.18-μm standard CMOS technology with newly proposed techniques. The VGA uses a cascode structure and the proposed wideband negative capacitance to realize a wide bandwidth.   The PD uses an improved unbalanced source coupled pair with an output differential amplifier and the proposed sink current steering to improve sensitivity. The VGA has a gain control range of -28~23dB and an input P1 dB of -33~-6dBm with a 3dB gain bandwidth of 1GHz. The PD has an input power range of -30~-20dBm with negligible Vout error over 0.1~1GHz. Finally, the proposed AGC circuit realizes an input dynamic range of -48~-8dBm and an operating bandwidth of 0.1~1GHz. The overall current consumption is 7.7mA under 1.5V supply.

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