# High-Efficiency Power Amplifier Using Novel High-Speed Bias Switching

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Dynamic bias switching is one of the practical solutions to the high-efficiency amplifications of the high-PAPR signals. There, however, are some problems in implementing the bias switching power amplifier. Two dc sources are required in order to switch the drain bias at two stages. Furthermore, a high-speed low loss switch is necessary for controlling the wideband signal envelope adaptively.

This paper presents a power amplifier with a noble high-speed drain bias switching. The proposed bias switching controller is different from conventional one in that it requires only one dc source.

Fig.1 shows an input signal waveform of the power amplifier and the dc drain bias according to it. Unlike the envelope following system, there are two dc bias states, high voltage ($V_H$) and low voltage ($V_L$). The drain bias of the PA is $V_H$ only when the input signal forms peak. Except the peak timing, the power amplifier operates at drain bias of $V_L$. Because the possibility that the RF peaks are generated in high-PAPR system is low, the overall efficiency of the PA using the bias switching technique is improved dramatically.

The above two voltage states can be generated using the combination of class E amplifier and the class E rectifier. Fig.2 shows the schematic of a high-speed drain bias switching circuit. When the control signal in Fig. 2 is high, the class E amplifier starts to operate and the output of it is rectified. In this case, the voltage of the load reaches to $V_H$. While the control signal is low, the class E amplifier turns off and the dc source ($V_{DD}$) is connected to the load through the diode. As the voltage drop of the diode is critical for efficiency of the bias switching circuit, the schottky diode is used. Therefore, load voltage ($V_L$) at low control signal is lower than $V_{DD}$ by 0.4V. The switching frequency of the class E amplifier is selected about 200MHz considering the switching speed and the size of the circuit.

Fig.3 shows the schematic of the proposed controller. When RF peaks of the system input are detected, the control signal in Fig. 3 is high and the drain bias of the main PA increases to $V_H$ from $V_L$. The main PA is biased class A, and $P_{1dB}$ is about 29dBm at 2GHz. Two-tone test is performed in order to measure the efficiency of the bias switching circuit. Tone space of the two-tone is 1MHz. Measured waveform of the drain voltage is shown in Fig. 4. The measured $V_H$ and $V_L$ are 5.2V, 2.6V each other. In these cases, the efficiencies of the bias switching circuit are 68% and 88% respectively.

The overall efficiency of the system depends on a probability of signal envelope, $V_H/V_L$, and efficiencies of the bias switching circuit. Assuming the signal is OFDM format, the designed bias switching system can increase the overall efficiency by about 70% compared to a fixed drain bias PA system.

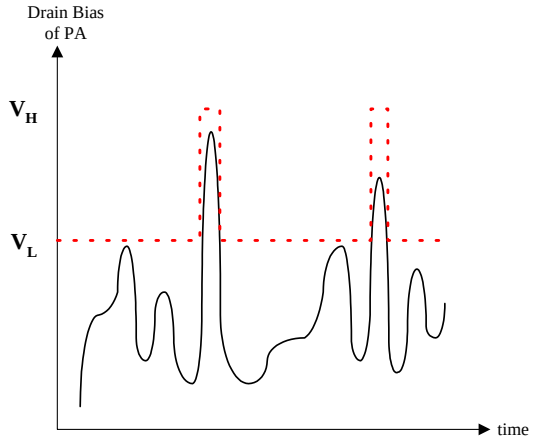


Fig.1. Input signal waveform of the power amplifier and the dc drain bias according to it

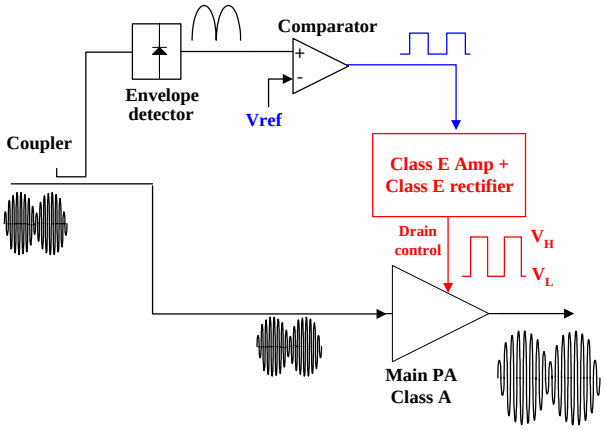


Fig.3. Schematic of the proposed controller

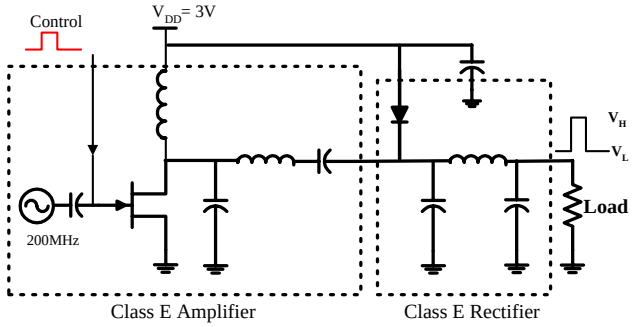


Fig.2. Schematic of the proposed high-speed drain bias switching circuit

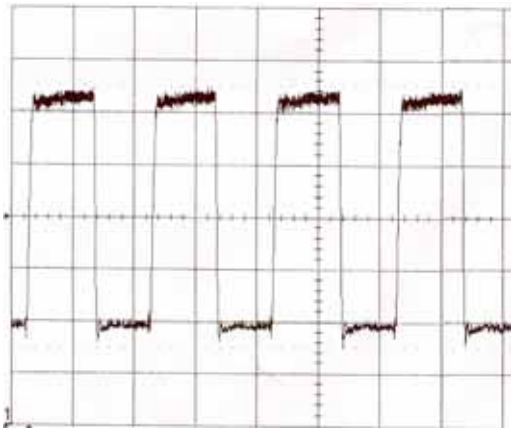

Fig.4. Measured waveform of the drain bias of the main PA when two-tone test is performed. Tone space of the two-tone is 1MHz