A Current-Mode FIR-Filter-Based Receiver Front-End For Blocker Filtering

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***Abstract* — A digital RF receiver front-end employing a FIR(Finite Impulse Response) filter is proposed for SAW-less receiver architecture, where the large out-of-band interferer can be rejected selectively by using a scalable frequency response property of FIR filter. The FIR filter, followed by the transconductor stage and current-commutating passive mixer, operates in current domain to improve the linearity. Also, the clock generator circuit can be simplified by making the FIR filter operate with 8-phase clock signal. The designed receiver front-end is fabricated using UMC 0.13 µm CMOS process. The chip shows unwanted blocker rejection over 80 dB, with good linearity of +3.94 dB IIP_3.**

***Index Terms* — FIR filter, digital RF, receiver front-end, blocker filtering, linearity.**

I. Introduction

As the number of wireless communication standard grows rapidly, the demand for mobile radio receivers is also increasing. In order to process various wireless standards, several single chip solutions which provide multi-mode/multi-band operation have been proposed recently [1]-[2]. The SAW-less receiver architecture is one of the most interesting topics in the multi-mode/multi-band or software defined radio (SDR) receiver systems. The elimination of the SAW filter makes it possible for the receiver system to operate with wide frequency bands. Without the SAW filter, however, in-band signals may be disturbed by large out-of-band interferers. What is even worse is the receiver may be saturated by these signals. Consequently, a method for rejecting out-of-band interferer near the in-band signal is needed.

In order to reject arbitrary interferer, the switched-capacitor based FIR filters have been actively researched [3]-[4]. The FIR filter structure is suitable for a low-pass type notch filter because it shows the *sinc* function frequency response. Moreover, using the frequency scaling property of the FIR filter, the notch frequency can be easily located. In case of rejecting the unwanted interferer with FIR filter, both the in-band signal and the out-of-band interferer should be amplified and fed to the filter linearly. For this reason, it is desirable to use current-mode rather than voltage-mode, which carries the risk of saturating the receiver system. However, since conventional FIR filters operate in voltage domain, a FIR filter that operates in current mode is proposed. The proposed filter accepts input as a form of current, and filtered output is in voltage domain.

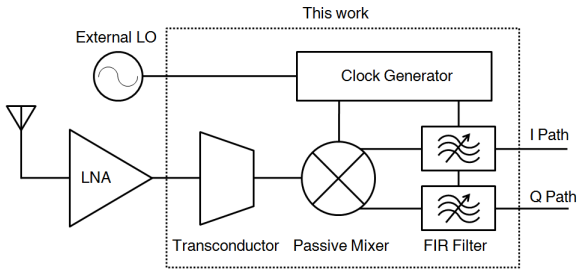

Fig. 1. The digital RF receiver front-end system architecture.

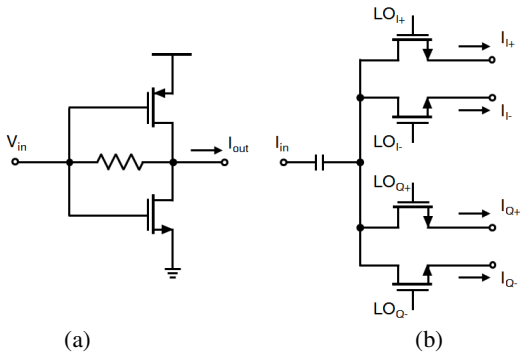

Fig. 2. Schematic of (a) transconductor and (b) current-commutating passive mixer.

II. Receiver Architecture

The proposed digital RF receiver architecture is shown in Fig. 1. The signal received by an antenna passes through low noise amplifier (LNA) and is amplified. The amplified voltage signal is fed to the transconductor amplifier stage and converted to the current domain. The current-commutating passive mixer downconverts the current domain signal to baseband and generates the differential I and Q quadrature signals. The current then flows into the FIR filter stage. The low-pass type FIR filters are based on the switched-capacitor circuits. The FIR filter response presents notch frequency controlled by the sampling frequency of the filter, so the unwanted out-of-band interferer can be rejected. The clock generator, which is circuit fed with external LO, supplies the LO signal to the mixer and the operating clock signal to the FIR filter.

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III. Circuit Implementation

A. Transconductor and Passive Mixer

Followed by an LNA, the transconductor stage converts the input voltage to current domain. By employing a simple inverter-based structure with a self-biasing resistor, the transconductor in Fig. 2(a) can convert both the input in-band signal and the out-of-band interferer linearly.

The current-commutating passive mixer in Fig. 2(b) downconverts the RF signal to the baseband. This mixer consists of four nMOS transistors operating as switches, which is turned on and off by four-phase clock generator signal. Using this zero-IF passive mixer, downconversion can be done with high linearity.

B. Current-mode FIR filter

The differential I and Q baseband signals from mixer are filtered in the current-mode FIR filter stage. Unlike the other FIR filter structure, this proposed FIR filter operates in current domain.

To compare the structure of the two filters, the conventional filter is checked firstly. The circuit schematic and clock configuration of the conventional 4-tapped FIR filter is shown in Fig. 3(a). Conventional FIR filters operating in voltage domain use a charge sharing method for filtering. When the input voltage is sampled by the switched-capacitor pair, the charge sharing operation produces the output voltage in C_{out}. In this moment, capacitors C_1 to C_4 and C_{out} are connected in parallel, and thus they will have the same voltage.

In contrast, the current mode FIR filter shown in Fig. 3(b) operates differently. Unlike the case of voltage input where the input voltage is sampled and held, current input is *integrated* during the time over which the switch turned on. In other words, the voltage mode filter generates charges on each capacitor, which depends on the amplitude of the input voltage, whereas the current mode filter generates voltages on each capacitor, which depends on the amount of the input current. Thus, to implement the current-mode FIR filter, the voltages on the capacitor, not the charges on them, need to be averaged.

To accomplish voltage averaging, the voltage buffer circuit is applied in each sampling path. When the current integration on each sampling path is complete, the average voltage of four paths is stored in the output capacitor.

The ideal 4-tap FIR filter frequency response and the designed 4-tap current-mode FIR filter frequency response are shown in Fig. 4. The comparative results show that the current-mode filter can effectively reject the unwanted interferer.

IV. Measurement Results

The designed receiver system is fabricated using an UMC 0.13 μm CMOS process. The die size is 1200 μm × 1180 μm,

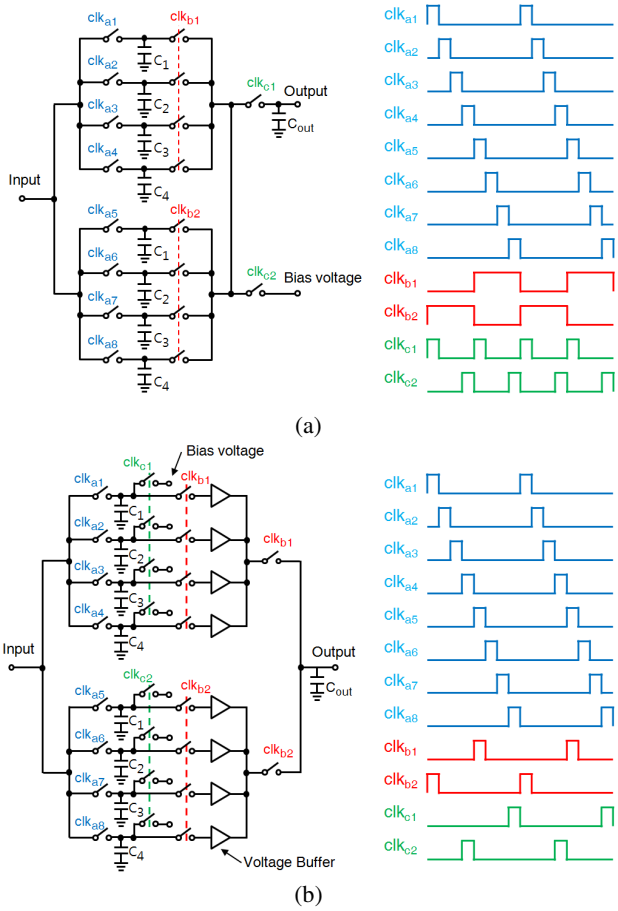

Fig. 3. Schematic and clock configuration of (a) conventional FIR filter and (b) current-mode FIR filter.

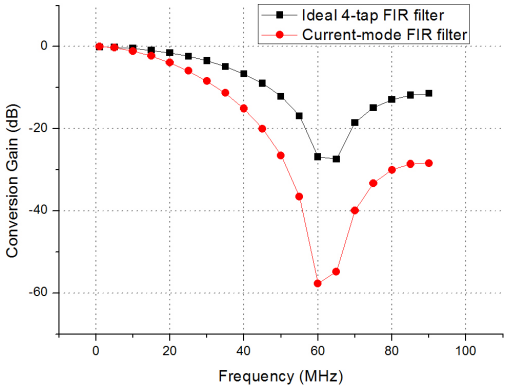

Fig. 4. Comparison of ideal 4-tap FIR filter with current-mode FIR filter frequency response.

and the active area of the chip is 800 μm × 650 μm in size. The photograph of the fabricated chip is shown in Fig. 5.

The receiver system is able to operate at a frequency range of 400 MHz to 1.2 GHz. In this section, the measurement results of a 500 MHz center frequency input signal and a 250 MHz FIR filter sampling clock speed are used.

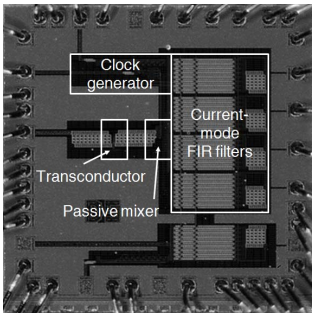

Fig. 5. Chip die photograph.

Fig. 6 presents the conversion gain of the receiver system. The input carrier frequency of 500 MHz is downconverted to DC, and the graph shows the filtering response at baseband. The conversion gain of the receiver at 1 MHz is −1 dB, and the −3 dB bandwidth is about 5 MHz. Due to the filter clock frequency of 250 MHz, notch frequency is located at 62.5 MHz. The measured result shows the receiver can reject the out-of-band interferer over 80 dB at notch frequency.

The linearity measurement was performed with a two tone test. Two tone signals (502 MHz and 503 MHz) are applied to the input, and the fundamental frequency at 2 MHz and the intermodulation term at 1 MHz are measured. The measured IIP_3 of +3.94 dB shows high linearity.

When measuring the single tone linearity test, an RF input signal at 501 MHz is applied to measure the in-band signal at 1MHz. The result shows P_{1dB} of −14 dB.

The noise figure of the system is calculated using gain method. The equation for obtaining the noise figure is as follows.

$$NF = P_{cold} - (-174) - 10\log B - G \qquad (1)$$

where P_{cold} is the noise floor when the input is terminated to 50 , B is the resolution bandwidth of the spectrum analyzer and G is the gain of the receiver front-end.

The calculated noise figure is 23.4 dB. The absence of LNA and the low gain of the receiver resulted in a significant drop on the noise figure. Increasing the transconductance gain would result better noise figure. The measurement result of the receiver front-end is summarized in Table I.

V. Conclusion

A digital RF receiver front-end with a current-mode FIR filter for blocker filtering is proposed. The frequency response scalable FIR filter is introduced to reject the unwanted out-of-band interferer. In order to the filter operate in current domain to prevent the receiver from being saturated, an FIR filter that uses a voltage buffer is designed. The fabricated receiver system consists of a transconductor, a passive mixer and the FIR filter stage. The measurement results show high blocker rejection with good linearity.

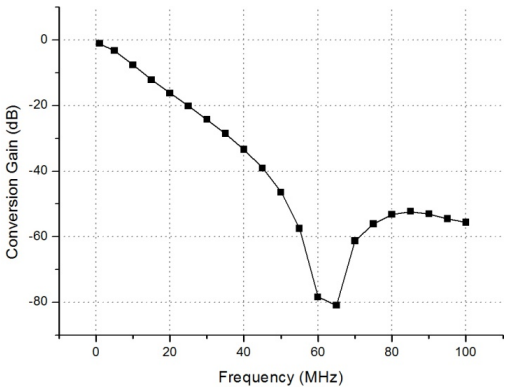

Fig. 6. Measured conversion gain of receiver front-end

TABLE I
Summary of Measurement Results

Parameter	Value
Gain (@ 1 MHz) [dB]	−1
Bandwidth [MHz]	5[a]
Attenuation [dB]	>80
IIP_3 [dBm]	3.94
P_{1dB} [dBm]	−14
Noise Figure [dB]	23.4[b]
Power Consumption [mW]	4.7
Active Area [mm^2]	0.52

[a] Filter sampling frequency of 250 MHz.
[b] External LNA is not included.

Acknowledgement

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