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([1]Yunnan University, [2]State Key Lab of Millimeter Waves of China, [3]University of Concordia, [4]University of Montreal, [5]University of Ottawa)

4. 17:10 – 17:30

A W-band Log-periodic Antenna for Millimeter Wave Applications

Hoang Anh Tuan, Yong-Hyun Baek, Sun-Woo Park, Sang-Jin Lee, and Jin-Koo Rhee (Dongguk University)

Session Active Component-2 (Chairs: Noriharu Suematsu, Hyunchang Park)

<Room B>

1. 08:40 – 09:00

A Low Power and Wide Locking Range Injection Locked Frequency Divider in 0.13 um CMOS

Hyang Hee Choi, Seong Jun Cho, Inn Yeal Oh, and Chul Soon Park (KAIST)

2. 09:00 – 09:20

Class-B Operation CMOS Power Amplifier for Millimeter Wave WPAN

Hiroyuki Nakase and Shuzo Kato (Tohoku University)

3. 09:20 – 09:40

Development of CMOS Circuits for Millimeter-Wave Phase Array System in 0.13 μm RFCMOS

Nguyen Bao Anh, Seong-Gwon Lee, and Jong-Wook Lee (Kyung Hee University)

4. 09:40 – 10:00

Design of An Efficient CMOS Power Amplifier Using Differential and Single-ended Power-combining Technique

Eunil Cho, Yonghoon Song, Sungho Lee, Joonlae Park, and Sangwook Nam (Seoul Nat'l University)

5. 10:00 – 10:20

K-band VCO and Injection Locked Frequency Divider in 0.13-μm CMOS Technology

Kyung-Hwa Yun, Seong-Kyun Kim, and Byung-Sung Kim (Sungkyunkwan University)

10:20 – 10:40 Coffee break

Design of An Efficient CMOS Power Amplifier Using Differential and Single-ended Power-combining Technique

Eunil Cho, Yonghoon Song, Sungho Lee, Joontae Park and Sangwook Nam

Institute of New Media and Communication, School of Electrical Engineering and Computer Science, Seoul National University, Seoul, 151-742, South Korea

Abstract **— This paper proposes an efficient power-combining architecture with differential and single-ended power amplifiers in a CMOS process. The single-ended amplifier is added for overall efficiency enhancement. To demonstrate this concept, a CMOS power amplifier using the proposed architecture is designed with a 0.13-μm CMOS technology that delivers 32.2 dBm of output power with 48% power-added efficiency at 1.95 GHz.**

Index Terms **— CMOS, power combiner, transformer, impedance transformation, power amplifier**

I. Introduction

CMOS power amplifiers have attracted a great deal of attention in recent years. The integration of radio frequency (RF) components including power amplifier (PA) is essential to realizing the true meaning of system-on-a-chip (SOC). In addition, PA is the most important component used to determine overall RF transmitter efficiency because it consumes the largest portion of DC power.

However, several factors deteriorate the performance of CMOS PAs. First, the low breakdown voltage of the transistor limits the output power. To overcome this problem, various combining approaches have been developed, such as the series stack method [1], and the transmission line based combiner [2]. Among them, a distributed active transformer (DAT) efficiently achieves a high output power and impedance transformation [3], [4]. Second, highly conductive substrates and thin metal layers reduce efficiency of on-chip passive devices. In spite of lossy on-chip passive characteristics, a transformer is a crucial component for implementing the power-combining architecture.

For these reasons, a watt-level CMOS PA using an on-chip power-combiner delivers the output power with relatively low efficiency. In this paper, a conventional power-combining method and the problem associated with CMOS PAs are briefly described. Then, an efficient power-combining method that alleviates the effects of lossy transformers is proposed and analyzed.

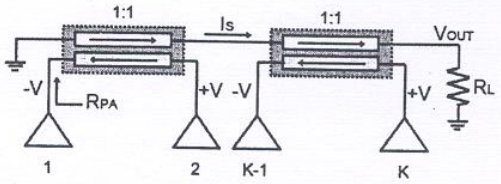

Fig. 1. Conventional distributed active transformer.

II. Power-Combining Architecture

A. Conventional DAT

The simplified architecture of distributed active transformers is shown in Fig. 1. It uses several 1:1 transformers to combine power. In this architecture, the identical AC voltage sources are arranged in series on the secondary part. Therefore, R_{PA} and the output power at the output terminal are related to the number of power stages. They can be calculated as

$$R_{PA} = \frac{V}{I_S} = \frac{R_L}{K} \tag{1}$$

$$P_{OUT} = K \cdot \frac{V_{DD}^{\ 2}}{R_{PA}} \tag{2}$$

As shown in (2), the output power is K times higher than one power amplifier using an ideal 1:1 transformer. Thus, this concept is one efficient power-combining method for a CMOS power amplifier with a watt-level output power. However, a shortcoming of this architecture is the low passive efficiency of each transformer. Actually, the maximum available gain (MAG) of the transformer is less than −1.3dB [5]. This can significantly degrade performance.

B. Proposed Architecture

Fig. 2 shows the new efficient power-combining architecture with differential and single-ended power

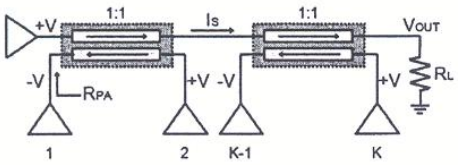

Fig. 2. The proposed architecture using an additional single-ended power amplifier.

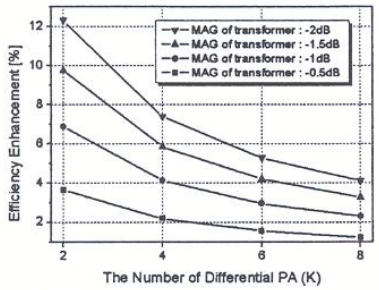

Fig. 3. Efficiency enhancement due to additional single-ended PA versus the number of differential PA for different MAG of transformers.

amplifiers. The role of single-ended power amplifier is to increase a portion of lossless power at the output. In the conventional architecture, the AC voltage sources suffering from a transforming loss are arranged in series. In the proposed architecture, one of them operates as a lossless voltage source due to the additional single-ended power amplifier. This concept can maximally enhance overall power efficiency. If power amplifiers consider ideal voltage sources, a simplified analysis of the circuit is similar to that of the conventional DAT.

$$V_{OUT} = (K+1)\cdot V \tag{3}$$

$$R_{PA} = \frac{V}{I_S} = \frac{R_L}{K+1} \tag{4}$$

Fig. 3 shows efficiency enhancement due to the additional single-ended power amplifier. In the case of lossy transformers, the proposed architecture presents greater enhanced efficiency than does the conventional architecture.

In addition, as illustrated in Fig. 3, better performance is exhibited when the minimum number of differential power amplifiers is used. Consequently, we can conclude

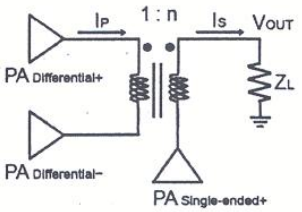

Fig. 4. The simplified circuit of the proposed architecture.

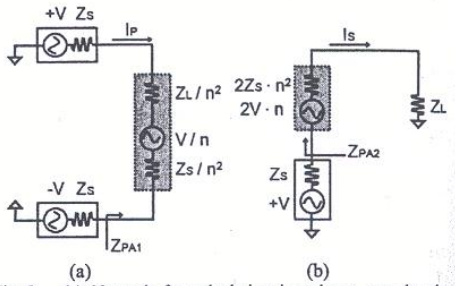

Fig. 5. (a) Network for calculating impedance seen by the differential PA. (b) Network for calculating impedance seen by the single-ended PA.

that the value of K is 2 for the large portion of lossless power at the output.

III. Analysis of Proposed Method

As seen in (4), with the assumption of an ideal voltage source, R_L is divided by the number of power amplifiers similar to equation (1). However, no power amplifier operates as a perfect voltage source. Thus, an analysis including source impedance of power amplifiers is needed, because that of single-ended power amplifier on the secondary path may cause asymmetry in the each R_{PA}.

Fig. 4 shows the simplified circuit of the proposed architecture, where K of the circuit shown in Fig. 2 is 2 and a turn ratio of the transformer is 1: n. Fig. 5(a) and (b) show the equivalent model for the transformer of Fig. 4, as seen in the active devices. The impedance seen by the differential power amplifier, calculated as the ratio between the current of the primary path and the output voltage of the PA can be derived as follows:

$$I_P = \frac{2V + \frac{V}{n}}{2Z_S + \frac{Z_L + Z_S}{n^2}}$$

$$Z_{PA1} = \frac{V - I_P \cdot Z_S}{I_P} = \frac{2Z_S + \frac{Z_L + Z_S}{n^2}}{2 + \frac{1}{n}} - Z_S \quad (5)$$

Based on these conditions, Z_{PA1} is computed as a function of not only Z_L, but also Z_S. However, where n is unity, Z_{PA1} is not affected by source impedance, Z_S.

$$Z_{PA1} = \frac{Z_L}{3} \quad (6)$$

A similar approach is used for the analysis of the secondary path case in Fig. 5(b), as follows:

$$Z_{PA2} = \frac{Z_S + 2Z_S \cdot n^2 + Z_L}{1 + 2 \cdot n} - Z_S \quad (7)$$

In addition, if it is assumed that n is 1 in equation (7), the impedance seen by the single-ended power amplifier and load impedance relation is

$$Z_{PA2} = \frac{Z_L}{3} \quad (8)$$

In summary, the proposed architecture has characteristics for impedance transformation similar to those of conventional DAT, where the additional reasonable design criterion is that transformers have a 1:1 transform ratio.

IV. Simulation Results

The proposed power-combining architecture for CMOS PA, including the driver stage and input balun, was designed using the 0.13-μm standard CMOS process. For high efficiency, a topology of the class-E switching PA [6], [7] was used in the power stage. The simulated power-added efficiency (PAE) versus supply voltage V_{DD} are plotted in Fig. 6 along with output power, at 1.95 GHz. V_{DD} varies from 1.2 V to 3.3 V, while other factors remained constant during the sweep. The amplifier achieved a PAE of 48 % at a maximum output power of 32.2 dBm according to operating frequency with a 3.3 V supply voltage of the power stage.

V. Conclusion

In this paper, a new power-combining architecture using differential and single-ended PAs has been proposed. The additional single-ended PA performs as a lossless power source. The analysis shows this structure provides an efficient impedance transformation. To demonstrate this concept, a 1.95 GHz CMOS power amplifier was designed with a 0.13-μm standard CMOS process. The amplifier shows a PAE of 48 % at a maximum output power of 32.2 dBm

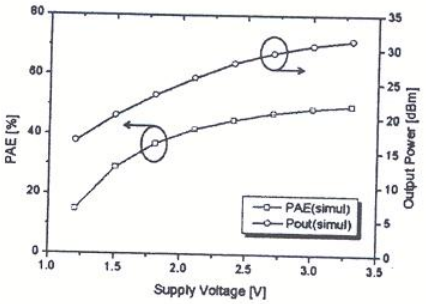

Fig. 6. The simulated PAE and output power versus supply voltage.

Acknowledgement

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