BRIEF PAPER

A 2.3–7 GHz CMOS High Gain LNA Using CS-CS Cascode with Coupling C

Hangue PARK[†a)], **Sungho LEE**[††], ***Nonmembers***, **Jaejun LEE**[††], ***Member***, ***and*** **Sangwook NAM**[††], ***Nonmember***

SUMMARY A fully integrated CMOS wideband Low Noise Amplifier (LNA) operating over 2.3–7 GHz is designed and fabricated using a 0.18 μm CMOS process. The proposed structure is a common source-common source (CS-CS) cascode amplifier with a coupling capacitor. It realizes both low voltage drop at load resistor (R_{load}) and high gain over 2.3–7 GHz with simultaneous noise and input matching and low power consumption. This paper presents the proposed design technique of a wideband LNA, and verifies its performance by simulation and measurement. This wideband LNA achieves an average gain (S21) of 16.5 (dB), an input return loss (S11) less than −8 dB, a noise figure (NF) of 3.4–6.7 dB, and a third order input interception point (IIP3) of −7.5–3 dBm at 2.3–7 GHz with power consumption of 10.8 mW under 1.8 V VDD.

key words: *wideband LNA, coupling capacitor, common source-common source cascode*

1. Introduction

Wideband LNA is one of key components in the receiving module of modern wireless wideband communication systems. It entails several design challenges due to the difficulty of wideband realization of the simultaneous input and noise matches, low power consumption, and high gain.

Therefore, several techniques have been proposed for the design of a wideband CMOS LNA such as Distributed LNA [1], Feedback LNA [2], Common Gate (CG) LNA [3], and Common Source-Common Gate (CS-CG) cascode LNA [4], [5]. However, Distributed LNA has a critical weakness of high power consumption and Feedback LNA has a large intrinsic noise due to feedback resistor. Also, CG LNA shows high noise figure because minimum noise figure of CG amplifier is higher than that of CS amplifier.

CS-CG cascode LNA shows a good performance in power consumption and noise figure. However, it still has a difficulty to realize high gain. Thus, we propose a new structure using CS-CS cascode (two stacked CS amplifier [6]) with coupling C (Fig. 1). This structure enables high gain with low power consumption and low noise figure. In the following sections, we will describe the proposed design in detail.

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[†]The author is with Telecommunication R&D Center, Samsung Electronics Co., Ltd., Suwon 442-600, Korea.
[††]The authors are with Seoul National University, Seoul, Korea.
a) E-mail: kami11@ael.snu.ac.kr

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2. Design

2.1 Structure Review

The CS-CG cascode is proper for the realization of wideband LNA due to its low power consumption and low noise figure over a wide frequency range [4], [5]. However, the CS-CG cascode has a gain limit for two reasons. First, large R_{load} to obtain the wideband flat gain causes a large voltage drop. Second, L_s and C_{ex} for input matching as shown in Fig. 2 lower the gain of the LNA because L_s decreases the voltage between gate and source of the FET and C_{ex} provides a route for high frequency bypass.

The CS-CS cascode structure offers a solution for the large R_{load}. It realizes a wideband flat gain not with a large R_{load} but with a stagger tuning technique. The comparison of the R_{load} is shown in Table 1. However the CS-CS cascode structure is still limited in realization of high gain if it still uses L_s and C_{ex} for input and noise matching [6].

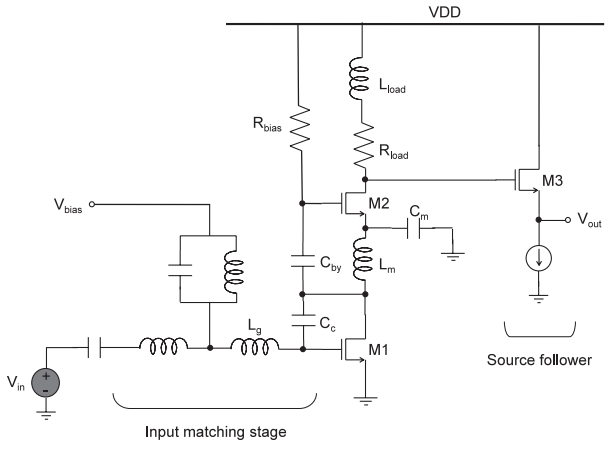

Fig. 1 Schematic of the proposed wideband LNA.

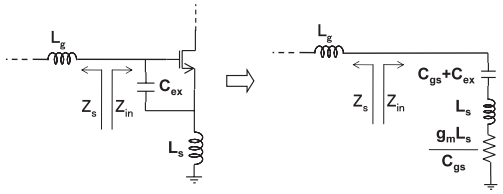

Fig. 2 Conventional narrowband input matching using L_s & C_{ex} and its equivalent circuit.

Table 1 Comparison of the 2nd stage load.

	This work (CS-CS)	[4] (CS-CG)	[5] (CS-CG)
R_{load}	25 Ω	90 Ω	90 Ω
L_{load}	2.6 nH	2.6 nH	3.0 nH

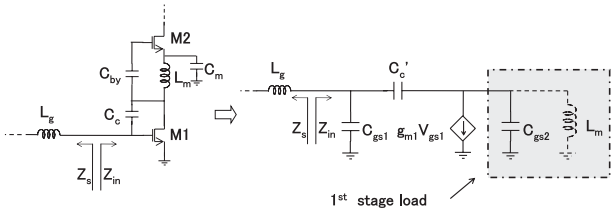

Fig. 3 Equivalent circuit for part of proposed CS-CS cascode with C_c.

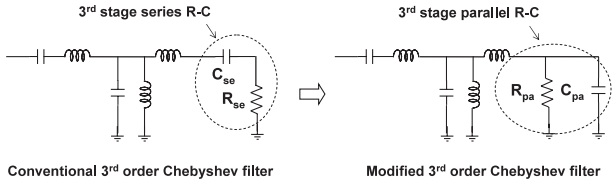

Fig. 4 Conventional and modified 3rd order Chebyshev filter.

So, we propose a new CS-CS cascode structure which uses coupling capacitor (C_c) instead of L_s and C_{ex}. The gain degeneration effect of C_c is much weaker than that of L_s and C_{ex} because C_c is so small (30 fF). Also, it enables simultaneous noise and input matching. In the next section, we will explain how the proposed structure realizes the simultaneous noise and input matching.

$$Z_{in} = \underbrace{\left(1 + \frac{C_{gs2}}{C_C'}\right)}_{\text{First term } (R_{in})} \cdot \frac{1}{g_{m1}} // \underbrace{C_{gs1} + \frac{C_C' \cdot C_{gs2}}{C_C' + C_{gs2}}}_{\text{Second term } (C_{in})} \tag{1}$$

2.2 Simultaneous Noise and Input Matching

Input impedance (Z_{in}) at the gate of M1 is found as an Eq. (1) from the FET small signal equivalent model as shown in Fig. 3. Each of C_{gs1} and C_{gs2} indicates the intrinsic gate-source capacitance of M1 and M2. Also, each of g_{m1} and g_{m2} indicates the transconductance of M1 and M2. C_c' indicates the sum of C_c and the intrinsic gate-drain capacitance of M1 (C_{gd1}). The load of M1 is simplified to

$$\begin{aligned} Z_{opt} &= \frac{\alpha\sqrt{\frac{\delta}{5\gamma(1-|c|^2)}} + j\left(\frac{C_{gs1}+C_{in}}{C_{gs1}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)}{\omega C_{gs1}\left\{\frac{\alpha^2\delta}{5\gamma(1-|c|^2)} + \left(\frac{C_{gs1}+C_{in}}{C_{gs1}} + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right)^2\right\}} \\ &= R_{opt} + jX_{opt} \end{aligned} \tag{2}$$

C_{gs2} because C_{by} and C_m are large enough to be considered as a short circuit and the L_m-C_{gs2} tank is considered as C_{gs2} for 2.3–7 GHz because LC resonance occurs around 2 GHz.

This parallel R-C equivalence of Z_{in} makes it possible to realize simultaneous noise and input matching because the parallel R-C can be implemented as the 3rd stage of the modified 3rd order Chebyshev filter as shown in Fig. 4. That is, R_{in} and C_{in} in Eq. (1) are implemented as R_{pa} and C_{pa} in the modified 3rd order Chebyshev filter.

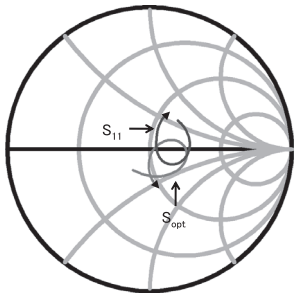

Fig. 5 Smith chart for $S11/S_{opt}$ of the proposed LNA over 2.3–7 GHz.

This modified 3rd order Chebyshev filter successfully replaces the conventional one by realizing appropriate values for R_{pa} and C_{pa}. We realized $R_{pa} \doteqdot 2.5R_{se}$ and $C_{pa} \doteqdot 0.5C_{se}$ which show the equivalence between each filter structure at the center frequency of 2.3–7 GHz. Also, these values for R_{pa} and C_{pa} result almost same quality factor for each filter structure. Accordingly, the S11 and S21 curves of the modified 3rd order Chebyshev filter follow those of the conventional one.

Now, let us discuss the procedure for the wideband power constrained simultaneous noise and input matching (wideband PCSNIM). In the design of a narrowband LNA, the PCSNIM technique using L_g, L_s and C_{ex} shown in Fig. 2 is widely used [7]. Also, this technique has been applied to the design of a wideband LNA as a wideband PCSNIM with the conventional 3rd order Chebyshev filter where L_g, L_s and C_{ex} are implemented as components of the filter [4], [5]. In a similar way, we can realize a wideband PCSNIM with the modified 3rd order Chebyshev filter using the proposed structure of CS-CS cascode with C_c. The entire design procedure consists of five steps as below.

1. Choose V_{gs1} to minimize NF_{min} at center frequency (f_c).
2. Choose W/L of M1 for required power consumption.
3. Choose C_c to make R_{opt}=R_{se} (50 ohm).
4. Choose L_g to make $X_{opt} = \omega L_g$ at f_c.
5. Choose W/L of M2 to make R_{in}=R_{pa}.

At step 1 and 2, we choose optimum V_{gs1} and W/L of M1 for minimum NF_{min} and intended power consumption. At step 3 and 4, we realize noise matching. The equation of Z_{opt} is shown in Eq. (2) with the predetermined device coefficients ($\alpha, \gamma, \delta, c$) [7]. First, we adjust R_{opt} to R_{se} (50 ohm) by tuning C_c. C_c is a dominant factor to determine R_{opt} because C_{gs1} and C_{ds1} are already fixed by W/L of M1 and $C_{gs2} \gg C_c$. Also, we adjust ωL_g to X_{opt} at f_c by choosing proper L_g value. Thus, Z_{opt} becomes equal to source impedance (Z_s). At step 5, we implement a modified Chebyshev filter to realize the wideband extension of noise matching as well as wideband input matching. We only need to adjust R_{in} to R_{pa} by W/L of M2 using Eq. (1) to implement a modified Chebyshev filter because C_{in} and L_g determined by step 1 to 4 are

automatically matched well for the filter. We verified this automatic matching by smith chart shown in Fig. 5. Note that this kind of automatic matching shows its efficacy in previous paper work for PCSNIM for CS-CG cascode LNA [7].

3. Simulation and Measurement Results

This section presents the simulation and measurement results of a wideband LNA operating at 2.3–7 GHz which is designed by the proposed technique of CS-CS cascode with coupling C. The proposed wideband LNA is fabricated using a 0.18 μm CMOS process and the die photograph is shown in Fig. 6. The IC was simulated using the Agilent Advanced Design System and tested using an on-wafer probe station.

Figure 7 shows the forward gain (S21) of 14.7–17.3 dB and Fig. 8 shows the noise figure of 3.4–6.7 dB. The average value of the forward gain is 16.5 dB and it is about 6 dB larger than the conventional CS-CG cascode LNA having S21 around 10 dB [4], [5]. Also the proposed LNA shows an input return loss (S11) of below −8 dB, reverse isolation (S12) of below −50 dB. Finally, IIP3 of the proposed LNA is measured to be −7.5 to 3 dBm with power consumption of 10.8 mW under 1.8 V VDD. The overall performance of the proposed LNA is summarized in Table 2 to be compared with the previously published papers.

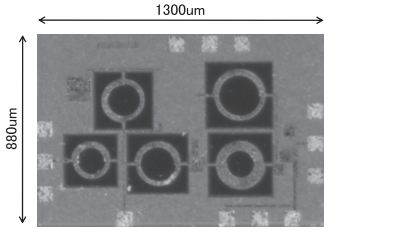

Fig. 6 Die photograph of the proposed wideband LNA.

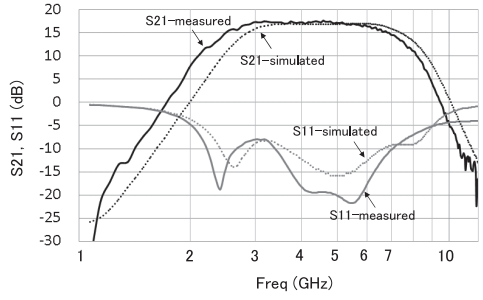

Fig. 7 Power gain (S21) and Input return loss (S11).

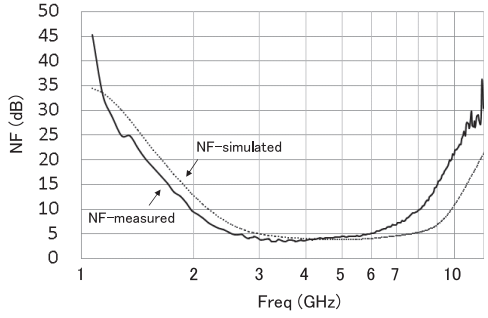

Fig. 8 Noise figure.

4. Conclusion

We proposed a new design technique of a CMOS wideband LNA with a CS-CS cascode structure with a coupling capacitor (C_c). This structure reduces the voltage drop at R_{load} by using the advantage of the CS-CS cascode and realizes a high gain by removing the source degeneration inductor (L_s) and external gate-source capacitor (C_{ex}).

We also verified the performance of the proposed wideband LNA through simulation and measurement. The measurement results agree with the simulation results well. The LNA shows high and flat gain as well as good input and noise matching over the 2.3–7 GHz frequency range. The high-gain with low-noise property of the proposed LNA can be useful in improving the system noise figure in wideband communication systems.

Acknowledgments

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Table 2 Summary of wideband LNA performance and comparison with previously published papers.

Specification	This work - measured	[1] - measured	[2] – measured	[3] - simulated	[4] – measured	[6] – simulated
Technology	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS
Topology	CS-CS cascode	Distributed	Feedback	CG	CS-CG cascode	CS-CS cascode
Frequency range (GHz)	2.3-7	0.6-22	2-4.6	3.1-10.6	2.3-9.2	2.6-9.2
Input return loss - S11 (dB)	<-8	<-8	<-8	<-9	<-9.9	<-11.5
Power gain – S21 (dB)	14.7-17.3	6.5-8.1	~9.8	15.9-17.5	~9.3	~10.9
Reverse isolation – S12 (dB)	<-50	<-43	N/A	N/A	<-43	N/A
Noise figure – NF (dB)	3.4-6.7	4.3-6.1	2.3-4	3.1-5.7	4-9	3.5-7.5
IIP3 (dBm)	-7.5@2.3G ~ 3@7G	N/A	-7@4.25G	N/A	-6.7@5G	-5.1@6G
Power consumption (mW)	10.8	52	12.6	33.2	9	7.1

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