LETTER
High Gain and Wide Range Time Amplifier Using Inverter Delay Chain in SR Latches

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SUMMARY This paper presents a time amplifier design that improves time resolution using an inverter chain delay in SR latches. Compared with the conventional design, the proposed time amplifier has better characteristics such as higher gain, wide range, and small die size. It is implemented using $0.13\,\mu$m standard CMOS technology and the experimental results agree well with the theory.

key words: time amplifier, time-to-digital converter, SR latch, high resolution delay measurement, all-digital phase-locked loop, inverter delay chain

1. Introduction

A time-to-digital converter (TDC), which quantizes time intervals between two rising edges, has been widely used in many applications such as space instruments and measurement devices [1], [2]. It has also been employed to measure the phase in an all-digital phase-locked loop (ADPLL) [3]. Since the resolution of TDC affects the performance of the system in most applications and the time amplifier (TA) determines this resolution, TA is one of the most important components of TDC. This paper proposes a TA design with improved time resolution by adding an inverter delay chain in the SR latch used in the conventional time amplifier. The proposed circuit is also robust to process variation.

2. Design

The prior TA shown in Fig. 1(a) has two SR latches with the characteristics of metastability. From the metastability, the output time difference T_{out} is derived by the input time difference T_{in} and the time offset T_{off} as shown in (1)–(3).

$$T_{out} = \tau \cdot [\log(T_{off} + T_{in}) - \log(T_{off} - T_{in})] \tag{1}$$

$$\tau = C/g_m \tag{2}$$

$$A_T = \frac{2 \cdot C}{T_{off} \cdot g_m} \tag{3}$$

where g_m is the transconductance of a NAND gate in metastability, C is the capacitance at its output, and A_T is the time amplifying gain [4], [5]. From (1)–(3), it should be noted that both the gain and the range of the input time difference can be controlled by the time offset T_{off} and NAND gate output total capacitance C in TA. Therefore, the proper time offset T_{off} that is constructed by the inverter delay chain
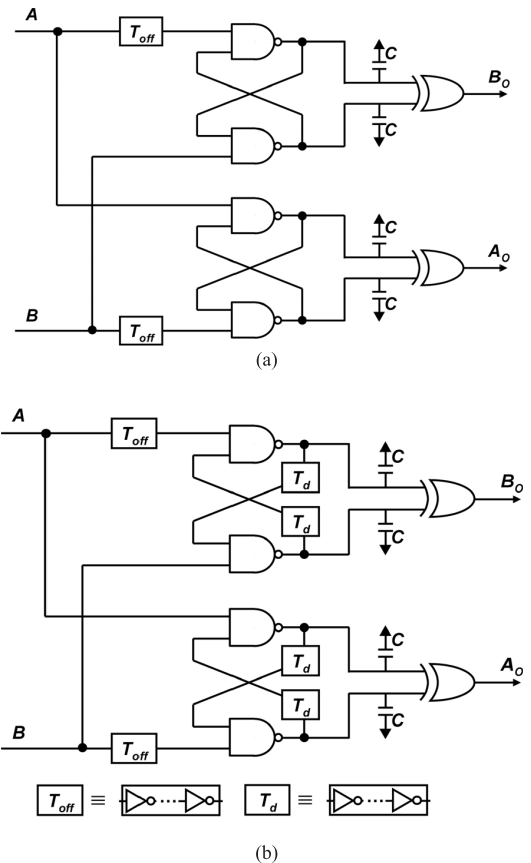
Fig. 1 (a) Prior time amplifier. (b) Proposed time amplifier.

and the extra capacitance added on the output NAND gate in the balanced SR latches can create a high gain A_T [5]. However, this method is very sensitive to process variation, and it is difficult to archive a fixed high gain and wide range, since the variation behavior of capacitance C and inverter delay T_{off} are different. In the case of adding another inverter delay T_d in SR latches as in Fig. 1(b), Eqs. (2) and (3) are converted to (4) and (5).

$$\tau = C/g_m + T_d \tag{4}$$

$$A_T = \frac{2 \cdot C}{T_{off} \cdot g_m} + \frac{2 \cdot T_d}{T_{off}} \tag{5}$$

From Eq. (5), added delay T_d improves A_T by $2T_d/T_{off}$ for the same capacitance C. In order for the prior TA to obtain a higher gain, a large capacitance with a large die area is required. However, a part of this capacitance can

be substituted by the inverter delay chain using (5), so that the die area can be reduced in the proposed design. Also, from Eqs. (3) and (5), we found that the proposed TA has higher gain than the prior TA in the same amplifying range T_{off}, and the proposed TA has wider range than the prior TA by $T_d * T_{off\,(the\,prior\,TA)} * g_m/C$ in the condition of the same amplifier gain. Therefore, we can design the high gain and wide range time amplifier.

In addition, A_T seems to have less process variation since the T_d and T_{off} shown in the second term in (5) are implemented by the inverter delay chains and have the same process variation. The delay of the inverter chain can be also adjusted by the current-starved circuit so that the gain of the proposed TAs can be controlled easily.

3. Simulation and Measurement Results

The proposed TA and the prior TA [5] were fabricated using $0.13\,\mu m$ CMOS technology. The chip micrograph is shown in Fig. 2. As shown in Eqs. (3) and (5), T_{off} controls not only the range but also the gain. Therefore, to compare the proposed TA with the prior TA in a fair manner, they were designed with the same amplifying range, T_{off} of 210 ps. In order to obtain a larger gain, a 311 fF MIM capacitor is added at the output of NAND in the prior TA, whereas a 106 fF MIM capacitor and inverter chain delay T_d of 120 ps are added in the proposed TA. The total area of the proposed TA ($62\,\mu m \times 30\,\mu m$) is approximately 54% that of the prior TA ($64\,\mu m \times 54\,\mu m$).

Figure 3 shows the simulation and the measurement data of the input time difference versus the output time difference graph. They agree relatively well and verify that the proposed TA has a better time amplifier gain with a small die area. The difference between the measurement and the simulation can be explained by the process variation of T_{off} and the NAND gate output parasitic capacitance. Moreover, the average dynamic current consumption of the proposed TA (0.50 mA) is smaller than the prior TA's (0.53 mA), according to the simulation. In addition, we measured three different die samples for process variation. As shown in Fig. 4, the proposed TAs show less process variation than the prior TAs. Therefore, the proposed TA can be expected the additional effect that is the process variation robustness.

4. Conclusion

A high gain/wide range time amplifier was proposed and fabricated using $0.13\,\mu m$ UMC CMOS technology. It realizes a higher gain with a smaller die area and process robustness compared with the prior TA. Although the proposed TA is designed for a bang-bang decision, it shows a meaningful gain improvement compared with the other proposed amplifier [5]. Improvement of the gain of the TA in a relatively wide range can be achieved by using the inverter delay chain in the SR latch. The proposed technique can be used for high resolution delay measurement.
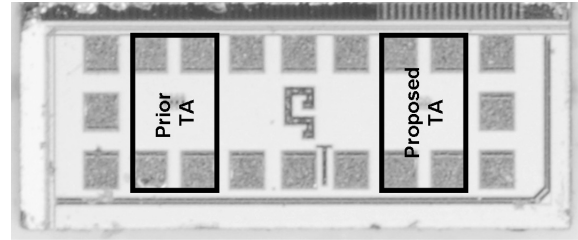
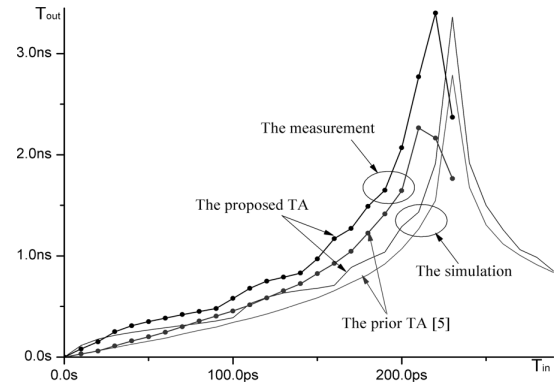

Fig. 2 Chip micrograph of the proposed TA.

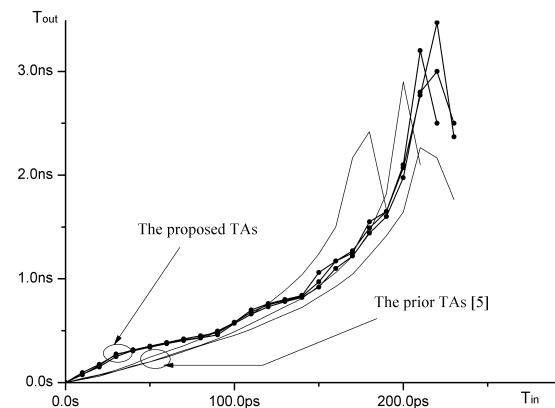**Fig. 3** Measured and simulated data of the proposed TA and the prior TA [5].

Fig. 4 Measured data of the proposed TAs and the prior TAs [5] from the three different die samples.

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