A Wideband Noise-Cancelling Receiver Front-End Using a Linearized Transconductor

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SUMMARY A wideband noise-cancelling receiver front-end is proposed in this brief. As a basic architecture, a low-noise transconductance amplifier, a passive mixer, and a transimpedance amplifier are employed to compose the wideband receiver. To achieve wideband input matching for the transconductor, a global feedback method is adopted. Since the wideband receiver has to minimize linearity degradation if a large blocker signal exists out-of-band, a linearization technique is applied for the transconductor circuit. The linearization cancels third-order intermodulation distortion components and increases linearity; however, the additional circuits used in linearization generate excessive noise. A noise-cancelling architecture that employs an auxiliary path cancels noise signals generated in the main path. The designed receiver front-end is fabricated using a 65-nm CMOS process. The receiver operates in the frequency range of 25 MHz–2 GHz with a gain of 49.7 dB. The in-band input-referred third-order intercept point is improved by 12.3 dB when the linearization is activated, demonstrating the effectiveness of the linearization technique.

key words: wideband receiver, transconductor linearization, noise-cancelling

1. Introduction

Recently, receiver architectures that can process multiple standards at different frequency ranges have been researched widely [1], [2]. Radar receivers that deal with dual-band input signals have also been researched [3]. These general-purpose receivers and radar receivers are designed without RF bandpass filters or surface acoustic wave (SAW) filters, which have limited bandwidth within a certain frequency range. The elimination of these filters is attractive since the receiver can operate over a wide frequency range; however, the absence of the filter allows the blocker signals to come into the receiver front-end. Large blocker signals may saturate the receiver circuits, or they may generate an intermodulation signal with the in-band signal. To prevent performance degradation in the wideband receiver front-end, passive mixers and low-noise transconductance amplifiers (LNTAs) are employed in [1] and [2]. The passive mixer is suitable for the wideband receiver since it has high linearity, and the LNTA can suppress the voltage gain at RF to prevent the circuits from being saturated. The basic architecture of the wideband receiver front-end is shown in Fig. 1.

Fig. 1 Basic architecture of the wideband receiver.

If a blocker exists, the linearity of the receiver becomes more important. When the blocker and the in-band signal are intermodulated, the intermodulation distortion arises. The amount of third-order intermodulation distortion (IMD3) components can be represented as an input-referred third-order intercept point (IIP3) value. To suppress the IMD3 and achieve high linearity performance, a linearization technique for a transconductor circuit is introduced [4]. This technique uses two-path feed-forward architecture, and the out-of-phase IMD3 components are added to cancel each other. Linearity can be increased by this technique, but additional circuits for linearization degrade the noise performance of the receiver. Therefore, a noise-cancelling technique [5] is used to reduce the noise.

In this paper, the wideband receiver front-end is designed using the linearization technique described in [4]. The noise-cancelling receiver architecture, including the linearized LNTA, is explained in Sect. 2. In Sect. 3, the measurement results of the fabricated circuit are presented. Section 4 concludes the paper.

2. Receiver Architecture

The basic architecture of the wideband receiver, shown in Fig. 1, consists of an LNTA, a passive mixer, and a baseband transimpedance amplifier (TIA). The LNTA converts the input voltage signal to a current with a transconductance of \(G_m\), and the passive mixer converts the RF current down to the baseband using local oscillator (LO) signals. To generate in-phase (I) and quadrature (Q) signals, a mixer driven by 25% duty-cycle LO signals is used. The baseband current is then converted into a voltage output in the TIA stage. The TIA consists of a high-gain operational amplifier and feedback resistors. By changing the feedback resistor value, transimpedance can be adjusted. This architecture is promising for the wideband receiver since the RF voltage swing is suppressed by the LNTA, and the risk of receiver...
saturation by the blocker signal can be reduced.

In the wideband receiver, the LNTA based on an inverter circuit is generally used. A simple inverter circuit consists of two MOSFETs of NMOS and PMOS, and this simple structure allows the inverter to operate at high frequency with minimal performance degradation. Yet, the inverter has high input impedance due to the gates of the MOSFETs. Since 50-Ω wideband input matching is necessary for the wideband receiver, high input impedance becomes a demerit.

To achieve the characteristic of wideband input matching, the global feedback architecture described in [5] is employed. Figure 2 shows a wideband receiver with global feedback. The negative feedback of the baseband current to the input node of the LNTA can accomplish 50-Ω input matching. The feedback resistor $R_{fb}$ adjusts the amount of feedback current from the baseband voltage output. With the feedback architecture, the input impedance $Z_{in}$ of the receiver becomes

$$Z_{in}(\omega_{LO} + \Delta\omega) \approx \frac{\pi}{2\sqrt{2}} \frac{R_{fb}}{1 + G_m \frac{\sqrt{2}}{\pi} Z_{BB} \Delta\omega}, \quad (1)$$

where $Z_{BB}$ is the transimpedance of the baseband TIA. Therefore, 50-Ω input matching can be achieved by adjusting $R_{fb}$ and $R_{TIA}$. Equation (1) also denotes that $Z_{BB}$ determines the shape of the receiver input impedance, which is close to 50 Ω at the center frequency, and reaches high impedance as the frequency offset $\Delta\omega$ increases.

The blocker signal is attenuated due to the high input impedance at the blocker frequency, but a larger blocker signal can still generate the IMD3 component at the LNTA output. To reduce the IMD3 component, a transconductor linearization method from [3] is adopted. Figure 3-(a) shows the wideband receiver with a linearized transconductor. As depicted in Fig. 3-(b), the linearized transconductor uses two-path feed-forward architecture to cancel the IMD3 component. In the main path, the input voltage is converted into a current by the transconductance of $2G_m$. In the auxiliary path, the input voltage is amplified by a voltage amplifier with a gain of $(-\sqrt{2})$ and converted into a current by the transconductance of $G_m$. If the transconductance is expressed with Taylor expansions, the relation of the input voltage and output current becomes

$$I_{out} = G_m V_{in} + G_m V_{in}^2 + G_m V_{in}^3 + \cdots. \quad (2)$$

The magnitude of the output current is normalized by linearization-off output current. When the linearization is turned on, the IMD3 component is reduced up to 30.5 dB, which proves that the linearization is effective. While linearity increases, the transconductance is reduced to $(2 - \sqrt{2})G_m$ as a trade-off.
The linearized transconductor is designed to have separate VDDs at each path. Therefore, when a large blocker signal exists, applying a VDD to the auxiliary path can make the linearization method activate (high linearity mode). For normal conditions without a blocker, the auxiliary path can be turned off (low noise mode).

Although transconductor linearization can be achieved by this method, the additional circuits used in linearization generate excessive noise. To improve the noise performance of the receiver, a noise-cancelling technique is adopted. Figure 5 shows the complete wideband receiver architecture with this noise-cancelling technique. An auxiliary path is added to the receiver in Fig. 3, and the second-stage TIA is added as a summation stage. In-band signals, which are applied to the inputs of LNTAs, are amplified and added in-phase at the summation stage. Noise signals generated in main-path circuits are fed back to the input node, and the polarity of the signal is reversed. This noise signal is sensed by the auxiliary-path circuits, so adjusting the auxiliary-path gain can generate a signal that has the same amplitude and reverse polarity as the original noise signal. Therefore, the noise signals at the TIA outputs of the main and auxiliary paths cancel each other.

A clock generator is designed to create LO signals for a four-phase mixer. To generate 25% duty-cycle non-overlapping LO signals, a divide-by-four circuit is implemented. The LO signals are generated by combining the outputs of the divider circuits.

3. Measurement Results

The designed receiver was fabricated using a standard 65-nm CMOS process. The chip die micrograph in Fig. 6 shows the chip size (960 μm × 650 μm) with pads.

Figure 7 shows the input matching characteristic of the receiver. As expressed in Eq. (1), optimum input matching of 50 Ω is achieved by adjusting resistor values. By changing the LO frequency, the $S_{11}$ values are maintained below −10 dB from 25 MHz to 2 GHz. Since the clock generator employs true single phase clock (TSPC) logic, it requires a reference clock frequency of 4 LO to create an LO signal. The high frequency clock requirement limits the mixer operation range.

The in-band gain and noise figure performance of the receiver is plotted in Fig. 8. For the gain measurements, an external amplifier was used to transform a differential baseband signal into a single-ended signal and drive a 50-Ω load. The external amplifier gain was de-embedded after this measurement. The maximum in-band gain is 49.7 dB, and the 3-dB cutoff frequency appears at 25 MHz for the lower bound and 2 GHz for the upper bound. The minimum noise figure achieves 5.1 dB when the linearization circuits are off (low noise mode).

The measurement is performed with an offset frequency sweep at the baseband. Figure 9 shows the gain, the 1-dB compression point (P1dB), and IIP3 measurement results. The single-tone of 1 GHz is applied to measure the gain and the P1dB. The 3-dB bandwidth of the conversion
Fig. 8  Gain and noise figure performance of the receiver.

Fig. 9  Gain, 1-dB compression point (P1dB), and IIP3 measurement results.

Table 1  Measurement results summary

<table>
<thead>
<tr>
<th>Topology</th>
<th>Noise Cancelling</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency (GHz)</td>
<td>0.025–2</td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>49.7 (Linearization off)</td>
</tr>
<tr>
<td>NF (dB)</td>
<td>5.1 (Linearization off)</td>
</tr>
<tr>
<td>Supply Voltage (V)</td>
<td>1.2</td>
</tr>
<tr>
<td>Current (mA)</td>
<td>16–24</td>
</tr>
<tr>
<td>IIP3 (dBm)</td>
<td>-18.39 (Linearization off)</td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>0.39</td>
</tr>
<tr>
<td>Process (nm)</td>
<td>65</td>
</tr>
</tbody>
</table>

gain is 9 MHz. The P1dB measurement results show a relatively low P1dB at the in-band due to the high level of gain, and the value increases as the offset grows. For the IIP3 measurement, the two-tone test is performed. The first tone at \( f_1 = f_{LO} + \Delta f \) and the second tone at \( f_2 = f_{LO} + 2\Delta f - 1 \text{ MHz} \) are applied to the input. This frequency setup always generates IMD3 components at 1001 MHz. Before the linearization circuits are turned on, the maximum IIP3 value is \(-18.39 \text{ dBm}\). When the linearization is turned on, the maximum IIP3 value is increased to \(-6.9 \text{ dBm}\); as shown in Fig. 9, the linearization method increases the IIP3 values up to 12.3 dBm. The receiver measurement results are summarized in Table 1.

4. Conclusion

In this paper, a wideband receiver using a linearized transconductor is proposed. A global feedback structure is applied to accomplish the wideband input matching. To enhance the receiver’s linearity performance, a linearization method that cancels the IMD3 components is adopted for the LNTA. Additionally, a noise-cancelling architecture is applied to reduce the excessive noise from additional circuits for linearization. The measurement results show the wideband characteristics of the receiver, and the significant improvement to IIP3 performance proves that the linearization method is effective.

Acknowledgments

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References