BRIEF PAPER

A 24 GHz Transformer Coupled CMOS VCO for a Wide Linear Tuning Range

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SUMMARY In this paper, a 24 GHz transformer-coupled VCO is presented for a wide linear tuning range in the 0.13-μm CMOS process. The measured results of the proposed VCO show that the center frequency is 23.5 GHz with 7.4% frequency tuning range. The output frequency curve has wide linear tuning region (5.5%) at the middle of the curve. Also, the VCO exhibits good phase noise of −110.23 dBc/Hz at an offset frequency of 1 MHz. It has a compact chip size of 430 × 500 μm^2. The VCO core DC power consumption is 5.4 mW at 1.35 V V_{DD}.

key words: *voltage controlled oscillator (VCO), wide linear tuning, transformer coupling, CMOS*

1. Introduction

In high-frequency applications such as radar sensors and communication systems, compound semiconductors are widely used due to their high cut-off frequency and high break-down voltage [1], [2]. However, with the increase in the demand for low-cost high-integration systems, CMOS has become an attractive solution. In the case of voltage-controlled oscillators (VCOs), it is great concern to design a CMOS VCO with low phase noise and a wide linear tuning range, as the VCO significantly affects the sensitivity and operating frequency range of a system which requires a fast tuning speed, such as radar systems [3]. However, conventional varactor-tuned CMOS VCOs suffer from nonlinear tuning range owing to inherent nonlinearity of the varactor capacitance [4]. To extend the linear frequency region, complementary VCOs which use both NMOS and PMOS cross-coupled pair are researched [5]. However, this structure struggles with output voltage swing limitation due to additional transistor cross-coupled pair. In this paper, by using transformer coupling, wide linear frequency tuning VCO is proposed.

2. Circuit Description

The proposed 24 GHz 1:1 transformer-coupled VCO circuit is shown in Fig. 1(a). Owing to the inherently low flicker-noise property compared to the NMOS counterpart [6], the cross-coupled pair and the tail current source are realized by PMOS. Figure 1(b) shows the designed 3-D stacked center-tapped 1:1 transformer. Its coupling coefficient is 0.83 at 24 GHz and its size is 138 × 121 μm^2. The primary and the

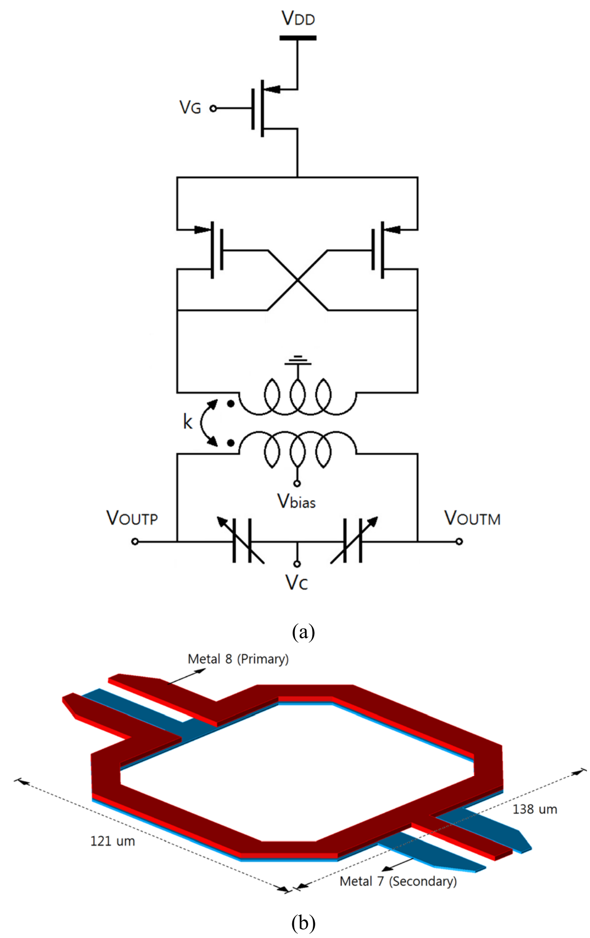

Fig. 1 (a) Schematic of the proposed transformer-coupled VCO, (b) 3-D stacked 1:1 transformer with center-tap.

secondary inductors of the transformer are connected to the VCO core and the varactor pair, respectively.

An advantage of utilizing the transformer coupling is extending the tuning range and the linear frequency tuning region of the VCO without generating an additional burden on the entire system such as the use of negative control voltage or higher control voltage than the system V_{DD}. The oscillation frequency of the varactor-tuned LC VCO is given as

$$\omega_{osc} = \frac{1}{\sqrt{LC_{tot}}}, \quad C_{tot} = C_{par} + C(V_F) \tag{1}$$

where C_{par} is the parasitic capacitance, $C(V_F)$ is the nonlinear varactor capacitance, and V_F is the forward bias across

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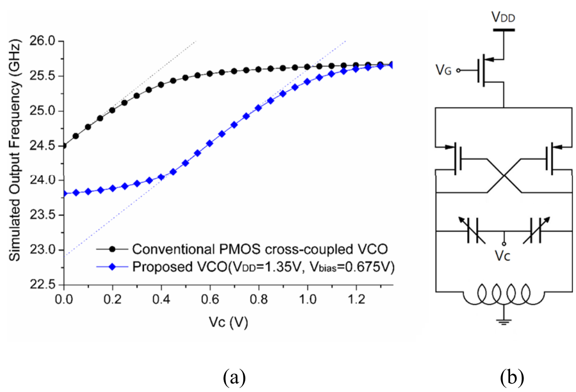

Fig. 2 (a) Simulated output frequency vs. V_C, (b) schematic of a conventional PMOS cross-coupled VCO.

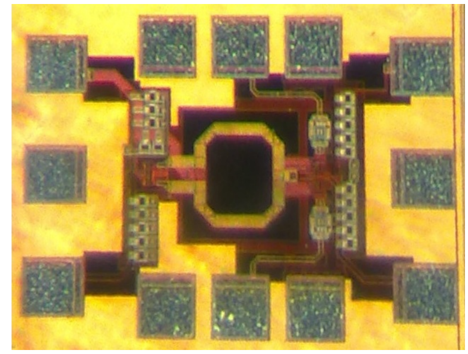

Fig. 3 Chip micro-photograph.

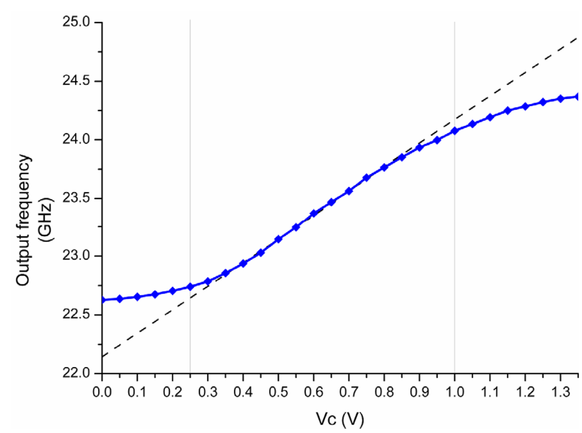

Fig. 4 Measured output frequency vs. V_C.

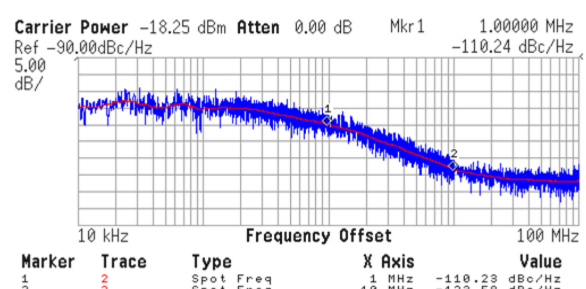

Fig. 5 Measured phase noise.

the junction, that is, the difference between the control voltage (V_C) and the common-mode level of the oscillation signal (V_{CM}). From (1), the oscillation frequency becomes a function of the difference between V_C and V_{CM}. It was noted that to maximize the linear tuning range of the VCO, it is necessary to set the transition point of the $C(V_F)$ curve (i.e., $V_F \cong 0$) in the middle of the available tuning voltage range, usually $V_{DD}/2$ [7]. This is accomplished when 0.675 V is applied to the center-tap of the secondary inductor (V_{bias} at Fig. 1(a)) in this VCO. Figure 2(a) shows the simulated output oscillation frequency of the proposed VCO [Fig. 1(a)] and conventional LC VCO [Fig. 2(b)] when the same-sized varactor is used. V_{CM} is 0 V in the conventional VCO; on the other hand, it is 0.675 V in the proposed VCO. The simulated frequency tuning range of the conventional VCO and the proposed VCO is 1 GHz and 1.75 GHz, respectively. Also the linear frequency region of the conventional VCO and the proposed VCO seems approximately 0.75 GHz and 1.3 GHz, respectively. It was found out that the tuning range and the linear region of the proposed VCO are much wider than those of the conventional VCOs. Furthermore, in systems based on a phase-locked loop (PLL) which is one of a core block of wireless communication systems and radar sensors, the actual operation range of the control voltage generated from a charge-pump of the PLL is typically narrower than 0 V~V_{DD} due to the drain-source voltage drop of the charge-pump transistors [8]. From this point of view, the proposed VCO can be a proper solution for the PLL based system because the linear frequency region appears at the middle of oscillation frequency curve.

3. Measurement Results

The proposed transformer-coupled VCO is fabricated in a standard 0.13-μm CMOS process. Figure 3 shows a chip micro-photograph. The chip size is $430 \times 500\,\mu m^2$, including the test pads. A simple common-source resistor load buffer is used. The measured output frequency is presented in Fig. 4. The center frequency and total tuning range of the proposed VCO are 23.5 GHz and 1.74 GHz, respectively, when V_C varies within 0 V~V_{DD}. The dashed-line is a tangent of the output frequency curve at the linear region. If the linear tuning region is arbitrarily defined by the region that the frequency error between output frequency curve and its tangent is smaller than 0.5% of each frequency, it is estimated at approximately 1.3 GHz (from 22.7 to 24 GHz) when V_C changes from 0.25 V to 1 V. The measured phase noise showed a feasible value of −110.23 dBc/Hz at a 1 MHz frequency offset [Fig. 5]. The core DC power consumption is 5.4 mW at 1.35 V V_{DD}. Table 1 details the performance comparison with published K-band CMOS VCOs. There is a work that shows better FOM_T than this work [12], however the linear frequency tuning range is not included in FOM_T. It is clearly found out that this work represents both decent FOM_T and the widest

Table 1 Performance Comparison with Published K-band CMOS VCOs.

Ref.	Technology	Center Freq. (GHz)	FTR (%)	Estimated Linear FTR (%) / Location of Linear Region	Phase Noise @ 1 MHz (dBc/Hz)	Core DC Power (mW)	FOM_T (dBc/Hz)
This work	0.13-μm	23.5	7.4	5.50 / center	-110.23	5.4	-187.7
[9]	0.13-μm	23	2*	0.60* / center	-100	4	-167.0
		23	1.5*	0.52* / center	-109.5	10	-170.5
[10]	0.18-μm	21.3	3*	2.67* / center	-105.9	9.6	-172.2
[11]	0.18-μm	18.95	3.58**	1.84** / edge	-110.82	3.3	-182.3
[12]	0.13-μm	24	9.4	4.58 / edge	-113	3	-195.5

*: Using negative tuning voltage, **: Using higher tuning voltage than core V_{DD}, $FOM_T = L\{\Delta f\} + 10\log((\Delta f / f_{osc})^2 \cdot P_{dc}) - 20\log(FTR/10)$

linear tuning region among the reference VCOs shown in above table. Also, this work can be a meaningful approach to PLL based systems since the proposed VCO has wide linear frequency region, and besides, the linear region appears at the center of the curve.

4. Conclusion

In this paper, a 24 GHz transformer-coupled VCO in 0.13-μm RF CMOS process is presented through, which it is possible to bias the core and the varactor-pair independently for an increase of the linear tuning range. The proposed VCO is thought to be quite useful in most of wireless systems and radar sensors due to the wide linear frequency tuning range which is located at the center of the frequency curve with simple structure.

Acknowledgments

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