An Adaptively Biased Class-C VCO With a Self-Turn-Off Auxiliary Class-B Pair for Fast and Robust Startup

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***Abstract*—In this letter, an adaptively biased class-C Voltage Controlled Oscillator (VCO) with a self-turn-off auxiliary class-B pair is presented for fast and robust startup in a 65-nm CMOS process. It consists of a main class-C core and an auxiliary class-B cross-coupled pair. The class-B auxiliary pair is used to solve the inherent startup problem of class-C VCOs. It works only during startup and turns itself off when the VCO reaches a steady state using an adaptive bias scheme. The dc current consumption of the VCO and bias circuit is 5 mA at 1.2 V V_{DD}. Here, a good phase noise level of -132.41 dBc/Hz at a 1 MHz offset frequency from a 2.46-GHz carrier is shown, to yield a Figure-of-Merit (FOM) of 192.45.**

***Index Terms*—Adaptive bias, class-B auxiliary pair, class-C, CMOS, self-turn-off, VCO.**

I. Introduction

RECENTLY, high-speed, low-power and low-noise CMOS systems have been widely developed due to advances in CMOS process and design methodologies of RF CMOS circuits [1], [2]. Achieving a low-power and low-phase-noise voltage controlled oscillator (VCO) is one of great concern because the VCO seriously affects the sensitivity of RF systems. Therefore, Class-C VCOs have been proposed steadily in recent years. Compared with an LC cross-coupled VCO, the class-C VCO provides better phase noise performance due to its low gate-bias voltage, which can be explained by impulse sensitivity function [3].

Given that a class-C VCO has inevitable startup problems due to its low gate-bias voltage, there have been several attempts to achieve robust startup such as hybrid VCOs [4], [5], a dual-conduction VCO [6], an adaptive bias scheme [7] and an automatic startup loop [8]. However, the hybrid and dual- conduction topologies, which are secure approaches for robust startup, are not sure solutions in that a free-running auxiliary pair distorts the class-C waveform and degrades the steady- state phase noise performance. A class-C VCO with the automatic startup loop shows good performance, but it has reliability issues because of its switching operation [9]. An adaptive bias scheme is generally considered to guarantee startup at the beginning of oscillation with a simple and small bias circuit.

To improve the startup beyond what an adaptive bias scheme can achieve a self-turn-off auxiliary Class-B pair that maintains low-phase-noise performance and mitigates the startup problem of class-C VCOs is proposed in this letter.

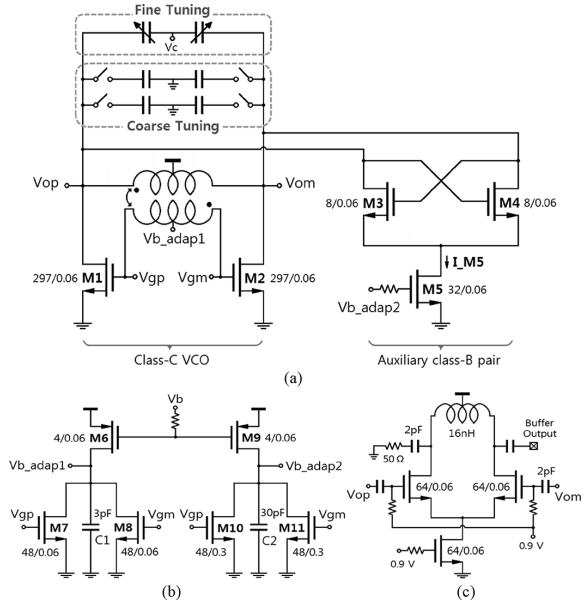

Fig. 1. (a) Schematic of the proposed class-C VCO with an auxiliary class-B pair, (b) the adaptive bias circuit, and (c) the output buffer.

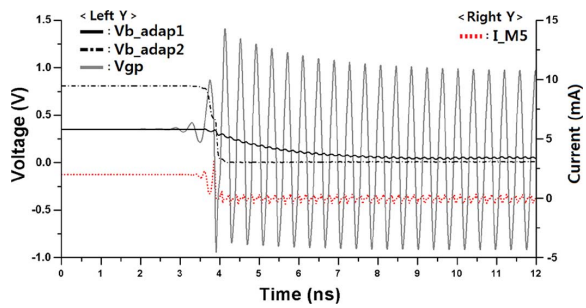

Fig. 2. Adaptive bias voltage waveform of the proposed VCO.

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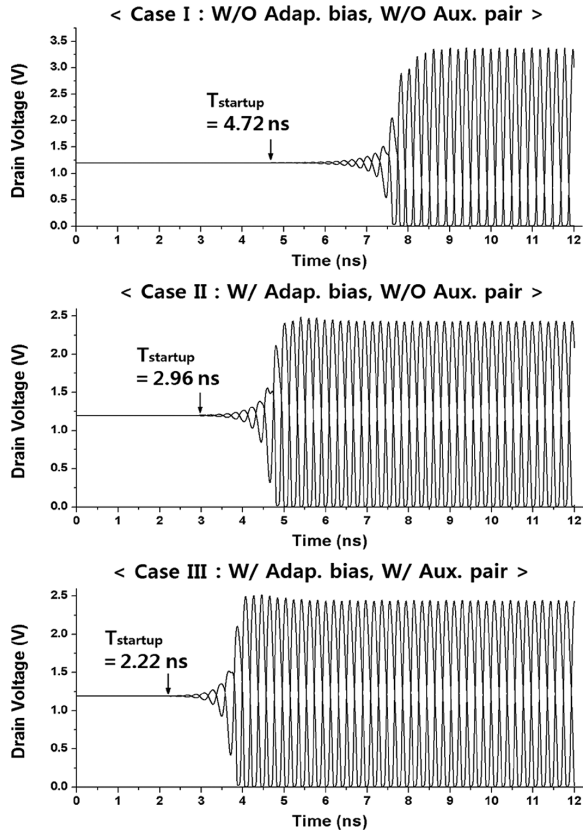

Fig. 3. Comparison of a class-C VCO startup by transient simulation.

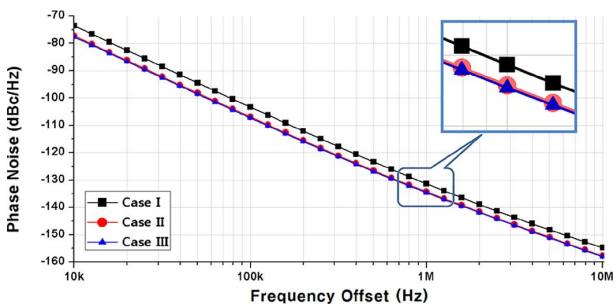

Fig. 4. Comparison of simulated phase noise of each case.

II. Proposed Circuit Description

A schematic of the proposed class-C VCO with a self-turn-off auxiliary class-B pair is shown in Fig. 1(a). The gate bias voltage of the main class-C pair (M1/M2) and that of the auxiliary class-B pair current source (M5) are generated by adaptive bias control circuits [Fig. 1(b)]. A bias network for class-C operation is simply realized by using the center-tapped secondary winding of a transformer, whose primary replaces the tank inductance [3]. The primary inductor has simulated inductance and quality factor (Q) at 2.5 GHz of 2.46 and 8.1 nH, respectively, and the secondary inductor has those of 1.66 and 6.4 nH, respectively. The coupling coefficient of the transformer is 0.86 at 2.5 GHz.

In the adaptive bias control circuit, the gates of M7/M8 are, respectively, connected to those of M1/M2 to mirror the M1/M2 currents. These currents are summed at the Vb_adap1 node and are compared with the M6 current. Then, the capacitor C1 converts the current difference to voltage. This voltage is fed back to the gate of M1/M2 through the center-tap of the transformer [7].

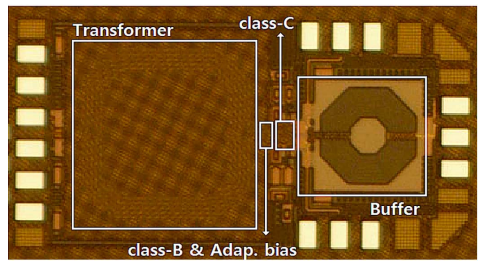

Fig. 5. Chip photograph.

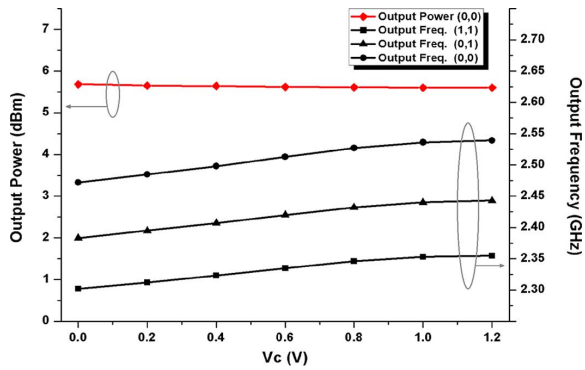

Fig. 6. Measured output frequency and output power.

TABLE I
Comparison of Startup Performance w/ & w/o the Self-Turn-Off Auxiliary Pair

w/o self-turn-off auxiliary pair		w/ self-turn-off auxiliary pair	
Core gate bias (V)	Tstartup (ns)	Core gate bias (V)	Tstartup (ns)
0.32	4.72	0.32	2.92
0.30	11.50	0.30	4.56
0.28	–	0.28	7.23
⋮	⋮	⋮	⋮
0.12	–	0.12	44.64
0.10	–	0.10	–

The transient waveforms of the class-C core and the adaptive bias circuit are shown in Fig. 2. The initial voltage and the slope of the Vb_adap1/Vb_adap2 graph are determined by the amount of current flowing in each bias circuit and by the sizes of C1 and C2. The initial voltage of Vb_adap1 is set to 0.32 V when Vb is 0.4 V to guarantee oscillation. With the increase in the voltage amplitude of the oscillator core (Vgp), the currents of the class-C core and the bias circuit are increased. This increased current of the bias circuit is integrated into C1 at the Vb_adap1 node and lowers the voltage of Vb_adap1 to nearly 0 V for class-C operation (the solid black line). The dashed black line in the graph shows the adaptive bias for self-turn-off operation. The gate of the current source (M5) is biased by 0.8 V to turn on M5 in an initial state and almost 0 V to turn it off in a steady-state. The simulated current of the auxiliary pair (the solid red line) in the initial state and the steady-state is 2 mA and nearly 0 mA, respectively. Therefore, the auxiliary class-B pair can provide an additional negative trans-conductance for

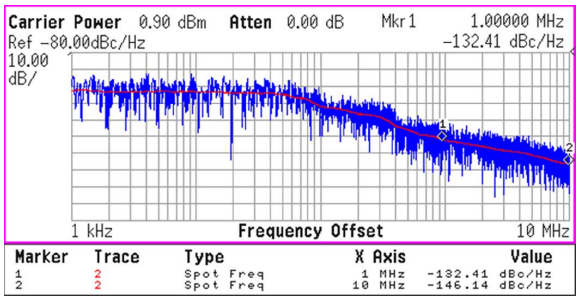

Fig. 7. Measured phase noise.

TABLE II
PERFORMANCE COMPARISON WITH PUBLISHED CMOS CLASS-C VCOS

Ref.	Topology / Techniques for startup	Freq. (GHz)	PN (dBc/Hz)	Core Power (mW)	FOM	Proc. (nm)
[3]	Class-C / None	4.9	−130 @ 3M	1.3	196	130
[4]	Class-B/C / Aux. pair (free running)	6.7	−137 @ 2M	27	188	55
[5]	Class-AB/B / Aux. pair (free running)	13.15	−101.4 @ 1M	2.4	180	180
[6]	Class-C / Aux. pair (free running)	5.4	−113 @ 1M	0.63	190	180
[7]	Class-C / Adaptive bias	5.1	−116.65 @ 1M	0.86	192.3	90
[8]	Class-C / Automatic startup loop	3.1	−123 @ 1M	1.57	191	180
This work	Class-C / Adaptive bias & Aux. pair (self turn off)	2.46	−132.41 @ 1M	6	192.45	65

$$FOM = -L(\Delta f) - 10\log\{(\Delta f / f_{osc})^2 \times P_{dc\_mW}\}$$

fast startup before entering the steady-state and then it turns itself off (no dc power consumption) in the steady-state.

Transient simulation results that verify the fast startup are shown in Fig. 3. In this work, $T_{startup}$ is defined according to the time when the difference between positive and negative voltage swings reaches 5 mV for the first time. The gate bias voltage of the VCO in case I is 0.32 V which is the same as the initial voltage of Vb_adap1 for a fair comparison. The startup time of the adaptively biased class-C VCO with the auxiliary class-B pair (Case III) is 2.22 ns, which is faster than that of the adaptively biased class-C VCO without the auxiliary pair ($T_{startup} = 2.96$ ns) as simulated in Case II and much faster than that of the general class-C VCO without a startup technique ($T_{startup} = 4.72$ ns), as also simulated in Case I.

The simulated phase noise of each case is shown in Fig. 4. Because the gate bias of the class-C VCO core is decreased adaptively (Case II and III), the current waveform of the VCO is sharper than that of Case I which provides a longer conduction time [7]. Therefore, the phase noise of Case II and III is lower than that of Case I as much as approximately 3 dB in simulation. Unlike conventional hybrid or dual-conduction topologies, the phase noise performance in Case III is not degraded compared with Case II because the class-B auxiliary pair which distorts the impulse-like class-C current waveform turns itself off in steady-state automatically. To verify how much the proposed self-turn-off auxiliary class-B pair contributes to the robustness of startup, the startup simulation results according to each fixed gate bias of the main VCO core are shown in Table I. The minimum oscillation gate bias voltage with and without the proposed auxiliary pair is 0.12 and 0.3 V, respectively. Thus, the self-turn-off auxiliary pair can guarantee oscillation when the initial voltage of the adaptive bias circuit is reduced by process variation or a mismatch of transistor models.

Judging from Figs. 3 and 4 and Table I, the proposed adaptively biased class-C VCO with the self-turn-off auxiliary class-B pair provides fast and robust startup without any performance degradation, such as phase noise increase or additional dc power consumption in the steady-state.

III. MEASUREMENT RESULTS

The proposed circuit is fabricated via a standard 65-nm CMOS process. Fig. 5 shows a photograph of a chip. The total chip size is $720 \times 1440\ \mu m^2$, including the test pads. The measured frequency tuning ranges are 2.30–2.36 GHz, 2.38–2.44 GHz and 2.47–2.54 GHz and the measured output power is approximately 5.5 dBm when the output buffer consumes 16.8 mW at 1.2 V V_{DD} [Fig. 6]. The output frequency and phase noise are measured by an Agilent E4448A spectrum analyzer with RF and dc probing. The measured phase noise shows a feasible value of -132.41 dBc/Hz at a 1 MHz frequency offset [Fig. 7]. The dc power consumption of the proposed VCO with the adaptive bias circuit is 6 mW at 1.2 V V_{DD}. Table II highlights the details of a performance comparison with recently published class-C VCOs.

IV. CONCLUSION

An adaptively biased class-C VCO with an auxiliary self-turn-off class-B pair for fast and robust startup was presented. The proposed VCO achieves fast and robust startup performances without degrading the phase noise performance or increasing the dc power consumption by using the self-turn-off auxiliary pair. Therefore, the proposed VCO shows excellent phase noise performance and FOM.

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