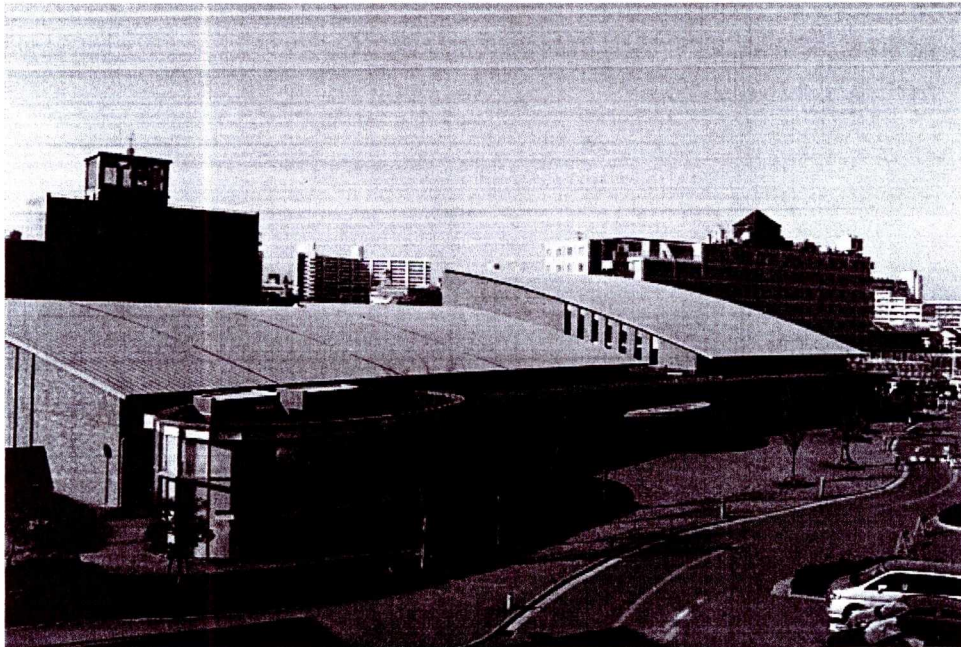


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# 2011 Korea-Japan Microwave Conference (KJMW 2011)

## Technical Digest



Kyushu University School of Medicine  
Fukuoka, Japan  
10-11 November, 2011

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## TH1-4: CMOS Circuits

Thursday, November 10<sup>th</sup>, 2011

Hall 1

**Session Chair** Kenjiro Nishikawa, Kagoshima University, Japan

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Kyushu University, Japan
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<sup>1</sup>Sungkyunkwan University, <sup>2</sup>Eltronix Co., Inc., Korea
- TH1-4-3** **Design of Wideband/High Efficiency CMOS Power Amplifier for Low Power Application** **70**  
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Junghee Choi, Jiyoung Chang, Sangwook Nam  
Seoul National University, Korea



# Design of Wideband/High Efficiency CMOS Power Amplifier for Low Power Application

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**Abstract** — In this paper, a novel low power amplifier for short range communication at 500MHz is proposed. It is designed and simulated in a standard 0.13μm CMOS technology. The proposed PA employs a bias current reuse and RF current combining structure and is designed to operate at Class C. Its drain efficiency reaches 68.4% at 500MHz while consuming only 2.7mW DC power from a 2.6 V power supply. And the efficiency maintains higher than 60% in 20% bandwidth of 450 - 550MHz, while output power difference is less than 3 dB in the same band.

**Index Terms** — CMOS power amplifier, current-combining, current-reuse, class C, low-power efficient amplifier

## I. INTRODUCTION

Recently, there is much interest on the research on a low-power system for a short range wireless communication. Its application range includes wireless personal area network (WPAN), wireless body area network (WBAN), wireless sensor network and so on. And many researches are on progress in various aspects like channel modeling, modulation method, etc. [1-6].

Especially a transceiver for biomedical applications is implemented and its performance was verified through experiments [7]. In the work, a simple type of power amplifier with a general structure is used, which operates in Class B. However it has several problems. First, additional transistor is needed to have a switching role to modulate RF signals. And the conventional structure has intrinsically limitation on the power efficiency in low power application since the supply voltage is too high for such a low power. Moreover, this type of PA should have high impedance transform ratio which results in the very narrow bandwidth.

To solve these problems, a novel type of power amplifier is suggested in this paper. In section II, a DC current-reuse and RF current-combining power amplifier which operates in class C is proposed, and its design procedure is explained. And in the next section, the simulation results in ADS are presented, which show PA's high efficiency and wideband characteristic. And a conclusion is in section IV. The design and simulation is in 0.13 μm CMOS technology provided by UMC.

## II. CIRCUIT DESIGN

### A. DC current reuse and RF current-combining Structure PA

A wideband power amplifier is implemented using current-combining structure. Generally, the optimum load impedance

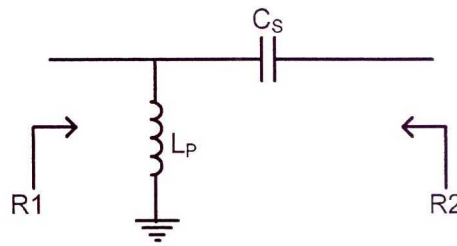


Figure 1 LC matching network for impedance transform

value for maximum output power should be transformed into the antenna's input impedance. When the ratio of two impedance values is lowered, the loss of the matching circuit is reduced. The relation of the transform ratio and Quality factor (Q factor) is shown below.

$$Q = \sqrt{\frac{R_1}{R_2} - 1}, \quad \text{when } R_1 > R_2$$

It is shown in the preceding equation that Q factor becomes lower if the transform ratio of matching circuit becomes smaller. Furthermore, it is known that the bandwidth becomes wider in the same situation. It means that high impedance and wide bandwidth are achieved simultaneously when the impedance transforming ratio is reduced.

To lower the ratio, the current-combining structure is used. It lowers the transform ratio by combining more than a couple of matching circuits in parallel, since an optimum load value is divided with the number of the composing circuits.

In the Figure 2, a power amplifier with the conventional structure and one with the current-combining structure are shown. While the current of N-power amplifiers are combined parallel at the output node, the amplitude of output voltage is lowered to one Nth of the conventional amplifier's. At the same time, the amplitude of output current is N times of the conventional amplifier's.

Therefore, the optimum impedance transform ratio of the PA structure (b) becomes  $1/N^2$  times of that of (a), as  $R_{opt}/N$  is transformed into  $N \cdot R_0$  in the circuit of Fig.2.(b), while  $R_{opt}$  is the optimum impedance of the Fig.2.(a)'s circuit, which is transformed into load impedance  $R_0$ .



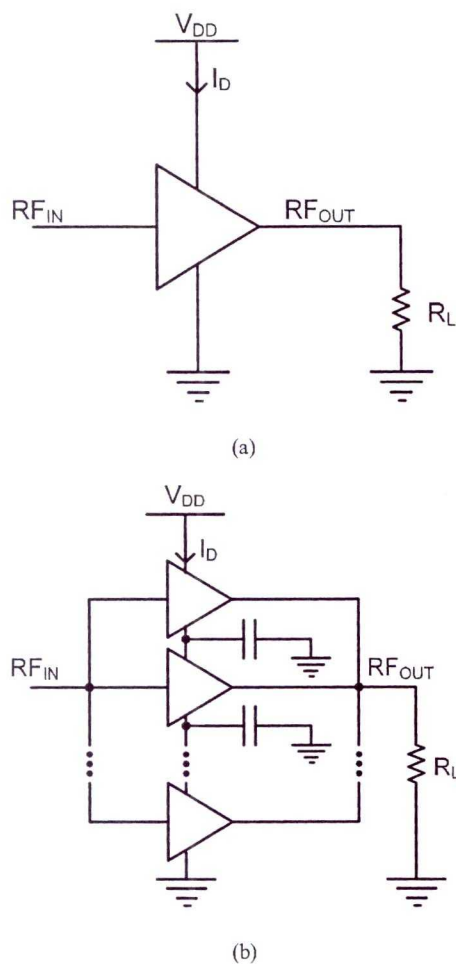


Figure 2 Structures of power amplifiers  
(a) Conventional power amplifier, (b) Current combining and current re-using power amplifier

Figure 3 shows that the schematic of the PA which consists of two-amplifier units employing current-combining and current-reuse structure that is proposed in this paper. In this structure, each amplifier gets the same input RF signal with a different offset. Load matching circuit is composed of parallel inductors and series capacitors.

Different from the conventional RF amplifiers, this circuit is designed for an antenna with 200ohm input impedance. Therefore, the power loss is reduced with lower Q factor than a conventional matching circuit which is designed to transform the optimum load impedance to 50ohm.

#### B. Implementation of Class-C PA

The proposed PA is designed for class C which has high efficiency with low PUF. Of course, the class D or E PA

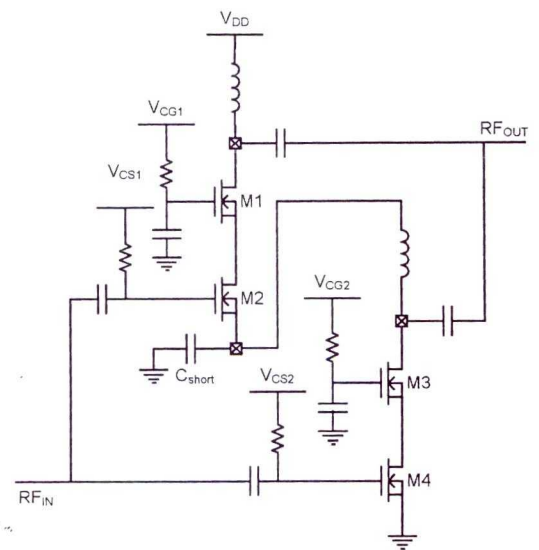


Figure 3 Schematic of the proposed PA

which is switching type amplifiers has higher efficiency than class C type. However, the switching PAs are narrow banded because they require not only LC series resonator but also additional matching circuit. Class-C PA has low conduction angles ( $<180^\circ$ ) so that the amplifiers cannot be used for high power applications. However, the drain efficiency is better than other linear PAs like class-A, class-B, and class-AB, so the class-C PA is proper to low power applications [8].

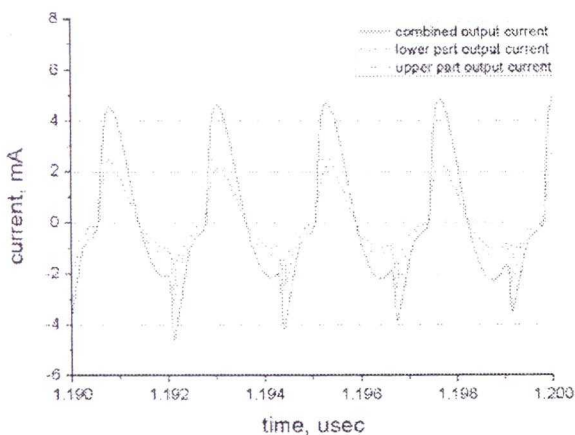
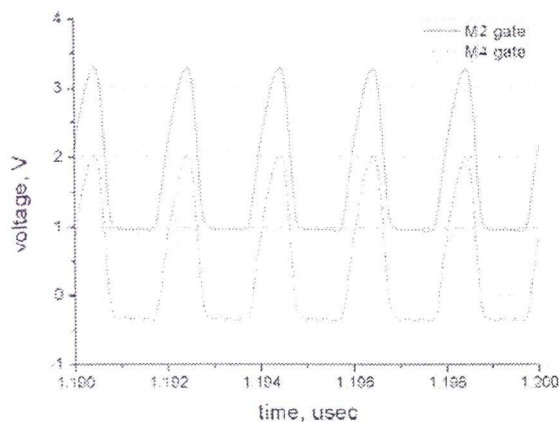
### III. SIMULATION RESULTS

The proposed low power current combining and current-reuse PA is designed and simulated in Advanced Design System (ADS) using a standard 0.13 $\mu\text{m}$  CMOS model provided by UMC. All of parasitic capacitors are considered in the simulation.

The input waveforms of the PA are shown in the Figure 4. They are made by the proceeding voltage controlled oscillator. The narrow pulse-waves are valid to make the PA operate in class C. And the output current waveforms are in Figure 5. It shows that the amplitude of the output current (the solid line) becomes twice by combining outputs of the top and the bottom part (the dotted lines) of this current-reuse structure.

The power gain is attained by measuring its input power, which is -17.8dBm at 500MHz. Since the output of power amplifier is 2.7dBm at the frequency, the power gain is about 20.5dB.

Figure 6 shows output power, power consumption, and drain efficiency with input signal's frequency from 400MHz to 600MHz. The peak to peak of the output power is less than 3dB in 450-550MHz range. In other words, the PA has the 3-dB bandwidth wider than 20%. Furthermore, the efficiency exceeds 60% in 450-550MHz range.



The designed PA's specification and simulated performance is summarized in the Table I.

#### IV. CONCLUSION

In this paper, a low-power amplifier is proposed and simulated in a standard 0.13 $\mu$ m CMOS technology. It is designed by employing the current combining and current-reuse structure and operates in class-C. According to the simulation results by ADS, the drain efficiency always maintains higher value than 60% between 450 and 550MHz. And the output power varies smaller than 3dB in the same frequency band which is valid range for spread spectrum modulation.

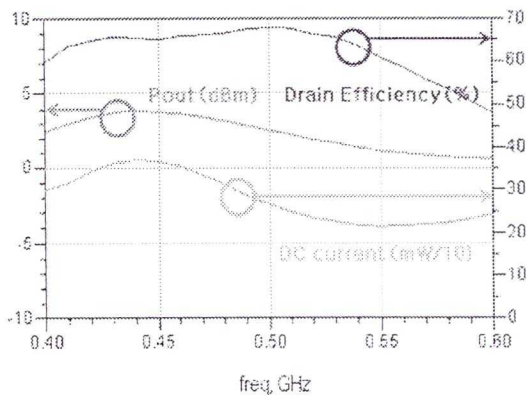


Figure 6 Drain Efficiency, Output power, and DC power consumption depending on frequency

Table I  
SPECIFICATION AND SIMULATION RESULTS (@  
 $f_c$ ) OF POWER AMPLIFIER

Technology	standard CMOS 0.13 $\mu$ m
Frequency ( $f_c$ )	500MHz
3-dB bandwidth	>100MHz
Supply voltage	2.6V
Output power	2.7dBm
Power gain	20.5dB
DC consumption	2.7mW
Drain Efficiency	68.4%
PAE	67.8%

#### ACKNOWLEDGEMENT

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