TABLE 1 Comparison of QVCO Performance

Ref.	CMOS Tech (μm)	Freq. (GHz)	V_{DD} (V)	P_{DC} (mW)	FOM (dBc/Hz)	Phase Error
[6]	0.18	1.1	1.8	5.4	−73.5	–
[7]	0.25	5	2.5	22	−185	0.26°
[8]	0.18	2.4	0.7	5.18	−185.35	1.9°
[9]	0.18	2.63	1.5	7.5	−176.4	–
[10]	0.18	1.88	1.8	3.6	−174.92	0.8°
[11]	0.18	6	1.8	5.76	−182.2	0.5°
This	0.18	5.44	0.6	2.4	−186.6	0.26°

been designed and implemented in the 0.18 μm CMOS technology, and it is designed to operate in the 5.44 GHz frequency band. The figure of merit for the proposed QVCO is −186.6 dBc/Hz. The QVCO shows phase noise of −115.62 dBc/Hz at 1 MHz offset from the oscillation frequency of 5.44 GHz while dissipating 2.4 mW for the whole QVCO from the supply voltage of 0.6 V.

ACKNOWLEDGMENTS

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A HIGH-EFFICIENCY POWER AMPLIFIER USING MULTILEVEL DIGITAL PULSE MODULATION

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ABSTRACT: *This article introduces a new architecture for a high-efficiency linear transmitter using a pulse modulated envelope signal. The transmitter employs multilevel PWM to represent the baseband signal. By using multilevel PWM, the efficiency of the power amplifier can be improved compared with that using the conventional PWM. To demonstrate the validity of the proposed architecture, a transmitter using three-level PWM is implemented and tested with the CDMA IS-95A signal. The measured PAE, including isolator and filter loss, is 37.6% at 21.6 dBm average output power and the linearity requirements are satisfied.* © 2009 Wiley Periodicals, Inc. Microwave Opt Technol Lett 51: 1921–1924, 2009; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.24494

Key words: *power amplifiers; switching mode power amplifiers; pulse modulation; PWM; multilevel PWM*

1. INTRODUCTION

In modern wireless communication systems, high-efficiency linear transmitters are needed to transmit data with less DC power consumption and smaller distortion. However, most of the linear power amplifiers compromise these two requirements: efficiency and linearity. To overcome this tradeoff, several methods have been proposed for linear power transmitter employing a nonlinear power amplifier (PA). The typical examples are polar transmitter, linear amplification using nonlinear components (LINC), and PA using digital pulse modulation [1]. In the case of the improved Kahn transmitter, a digital pulse modulated envelope signal is used to turn the switching amplifier on and off [2, 3]. A $\Delta\Sigma$-digitized polar transmitter, which is a modified form (drain switching) of PA using digital pulse modulation, was also proposed [4]. The latter has a simpler structure but AM/AM and AM/PM distortion make it difficult to achieve high linearity. The former can avoid these problems by mixing the pulse modulated signal with an RF phase signal and applying the pulsed RF signal to the gate of power transistors.

In this article, a multilevel digital pulse modulation technique is proposed for improved efficiency. Small input signals are modulated by lower amplitude levels, and their pulse width can be increased. This scheme reduces the total harmonic power of the modulated signal and results in improved efficiency. This can be implemented with either an improved Kahn transmitter or a polar transmitter type. The first type is used in this article.

2. MULTILEVEL DIGITAL PULSE MODULATION

There are several modulation methods for a pulse signal to represent varying envelopes, such as pulse width modulation (PWM), delta modulation, and Δ-Σ modulation. The conventional digital pulse modulation scheme uses only two amplitude levels, and the output power is controlled with the duty ratio (D) of the pulse signals. There is a relation between efficiency (η) and the duty ratio given by Eq. (1) [3].

$$\eta = D \cdot \eta_{PA} \tag{1}$$

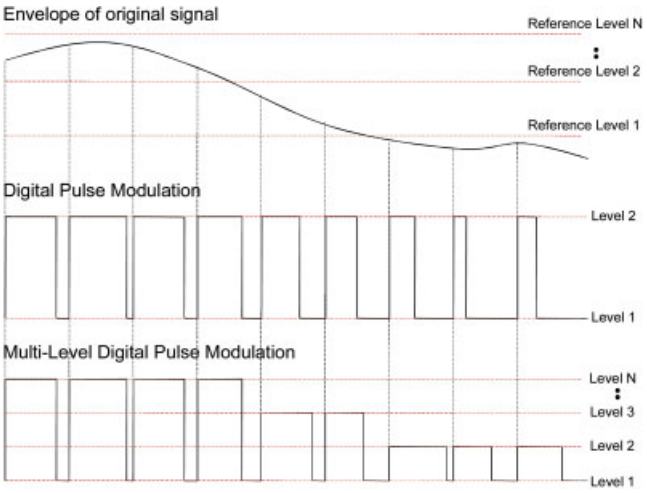

Figure 1 Concept of digital pulse modulation and multilevel digital pulse modulation. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

Since the efficiency is proportional to the duty ratio, narrow pulse signals lead to the degradation of efficiency. This can be mitigated by applying multilevel digital pulse modulation. The concept of multilevel digital pulse modulation is shown in Figure 1. It uses N amplitude levels. For small input signals, low pulse amplitude levels are selected and the duty ratio can be increased to maintain the same output power. As the number of levels, N, becomes larger, the total efficiency of multilevel digital pulse modulation increases. However, the implementation is more complicated for large N.

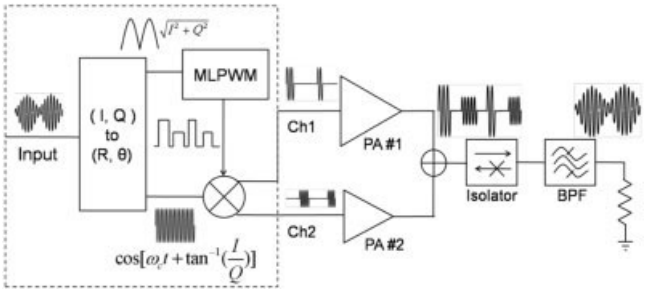

Figure 2 Block diagram of the proposed high-efficiency linear transmitter using three-level digital pulse modulation

In this article, a linear PA using three-level pulse width modulation (PWM) is implemented, which can be extended to multiple levels. Figure 2 shows a block diagram of the proposed architecture. The input RF signal is split into an envelope and a phase signal by a polar modulator, and the envelope is modulated by three-level PWM. The digitalized signal and the RF phase signal are mixed to generate the RF pulse train. The mixed signal is divided into a high level and middle level. A large PA amplifies the high level of the pulse signal and a small PA amplifies the middle level. After filtering the combined RF pulse signal using a band pass filter, the amplified RF signal is restored. An isolator is needed to prevent the reflected power of the band pass filter from causing a stability problem.

3. DESIGN OF THE PROPOSED ARCHITECTURE

For high efficiency, class E PAs are used for the amplifying devices. A class E PA is a zero voltage switching (ZVS) amplifier which is composed of a shunt capacitor and a series LC resonator [5]. These circuits modify the drain voltage and current waveforms so that they do not overlap; ideally, 100% efficiency can be achieved. However, because of the parasitic components in the switch, the performance degrades. In the on-state, a switch can be considered an on-resistance (R_{on}). In the off-state, it is equivalent to an output capacitance (C_p). Smaller R_{on} and C_p give higher efficiency. The size of the transistor has to be chosen carefully, as this determines R_{on} and C_p, and is also related to the operating speed of the PA. The class E PA usually has a high-peak voltage, so a transistor needs to have high-breakdown voltage to achieve high-output power. Figure 2 is a schematic of the implemented class E power amplifier. Passive components, including a matching network, are realized with microstrip transmission lines. An open stub and λ/4 line are designed to control the impedance at fundamental and harmonic frequencies.

A combining circuit is designed to have low loss using λ/4 transmission lines [6]. Figure 3 shows the schematic of the ideal combining circuit. Two PAs are connected with λ/4 transmission lines that have characteristic impedance of Z_0. Then, the input impedance becomes Z_0 for $R_L = Z_0$ since λ/4 lines have the input impedance of $Z_{in} = Z_0^2/R_L$. In addition, the output impedance of λ/4 lines is infinite because the source impedance is ideally zero. In this way, the ideal insertion loss of 0 dB can be achieved. In reality, the output impedance of a turned off PA is not zero, and it causes a power combining loss. The length of each λ/4 transmission line is adjusted to achieve the maximum Z_{out}. Furthermore, the characteristic impedance and length of the combined line is

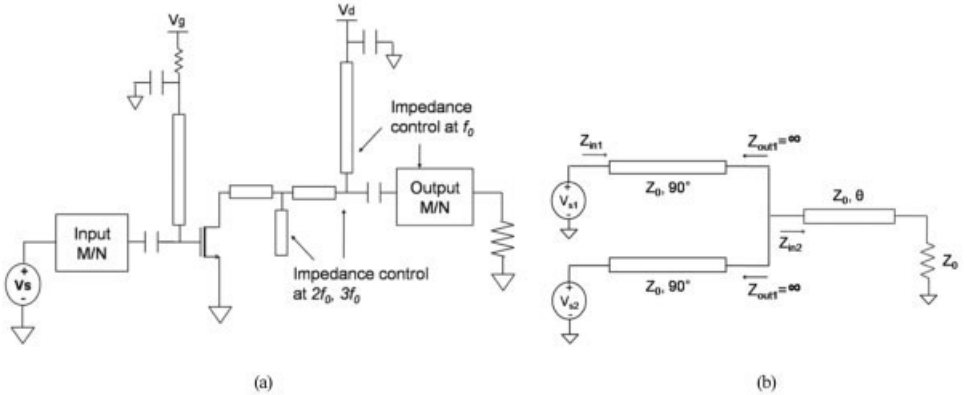

Figure 3 Schematic of the (a) class E power amplifier and (b) ideal combining circuit

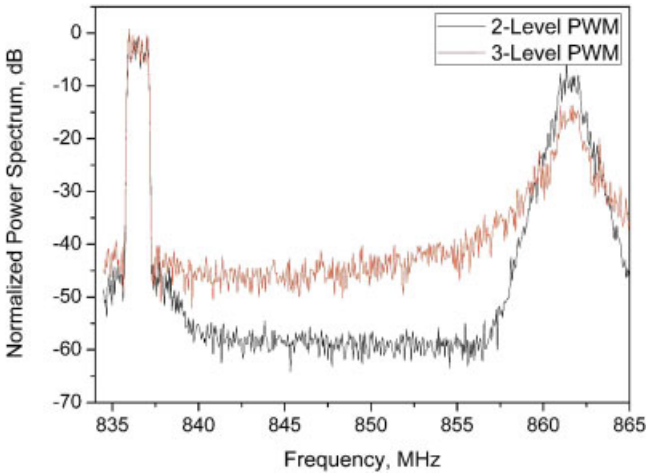

Figure 4 Measured spectrum of digital pulse modulated CDMA IS-95A signal. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

controlled to have $Z_{in1} = 50\ \Omega$ and smaller Z_{in2}. The fabricated combing circuit has 0.4 dB of combing loss.

4. MEASUREMENTS

The architecture using digital pulse modulation in Figure 2 is implemented with a combination of software programming and hardware measurements. The pulse modulation is achieved with MATLAB coding using CDMA IS-95A sources in the Agilent Advanced Design System. The modulated signal is generated using Tektronix's Arbitrary Waveform Generator AWG7102. Figure 4 shows a measured spectrum of the modulated signal. A 25 MHz sampling frequency is used for PWM and its harmonics are repeated at each integer multiple of the sampling frequency. If higher sampling frequency is used, harmonics are kept apart more distantly from the in-band signal. Then, it is possible to use a lower Q band pass filter, which has a smaller insertion loss. In Figure 4, a spectrum of three-level PWM is also plotted. As shown in the spectrum, the sum of harmonic power is lower, which means that there is an improvement in efficiency.

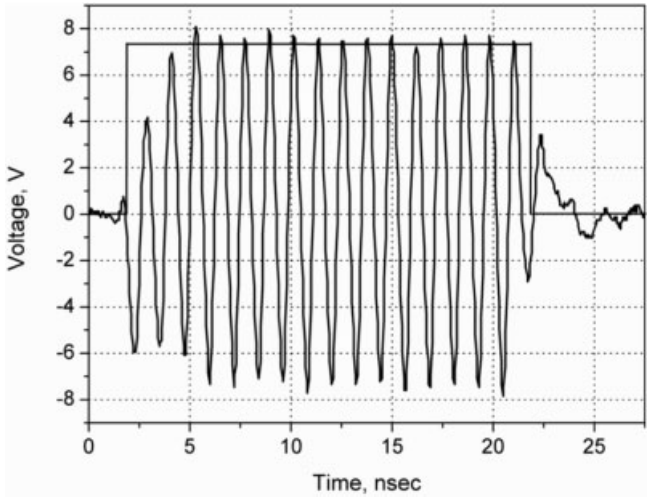

Figure 5 Time domain output signal with 25 MHz sampling frequency and 50% duty ratio

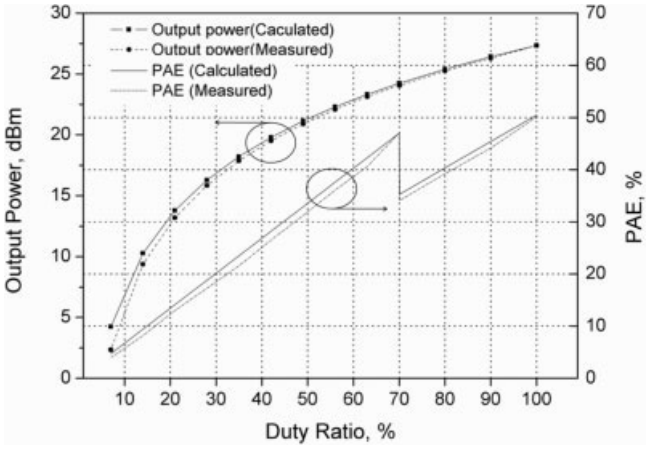

Figure 6 Measured PAE versus the duty ratio of RF pulse signal

4.1. Performance for RF Pulse Signals

A class E PA is implemented with EFA-480D, GaAs FET by Excelics. It has a relatively high-breakdown voltage and a small on-resistance. Rogers RO4350 with $\varepsilon = 3.43$, $h = 30$ mil, is used for the substrate. A PA is fabricated at 836.5 MHz for the amplification of the reverse link CDMA IS-95A signal. When it is operated with $V_g = -2.6$ V, $V_d = 6.1$ V, the measured PAE is 71% at 28 dBm continuous wave (CW) output power.

Figure 5 shows the time domain output signal of the PA when the RF pulse signal is applied at the input with 25 MHz switching frequency and 50% duty ratio. There is about 1 ns of rising time owing to the effect of passive components and the time required for the transistor to be turned on. Figure 6 shows the performance of an implemented PA when the RF pulse signal is used with a 25 MHz sampling frequency. There exists a little degradation in the measured results compared with the theoretical ones. This is considered to be caused by the distortion of the RF pulse signal. In addition, the PAE of the amplifier is reduced because of the insertion loss that occurs in the combining circuit, isolator, and BPF. As explained in the previous section, the efficiency is proportional to the duty ratio. In the implementation, signals under 70% are modulated by the middle level. When a small PA is being operated, PAE is 47% at 24.24 dBm; this decreases linearly as the

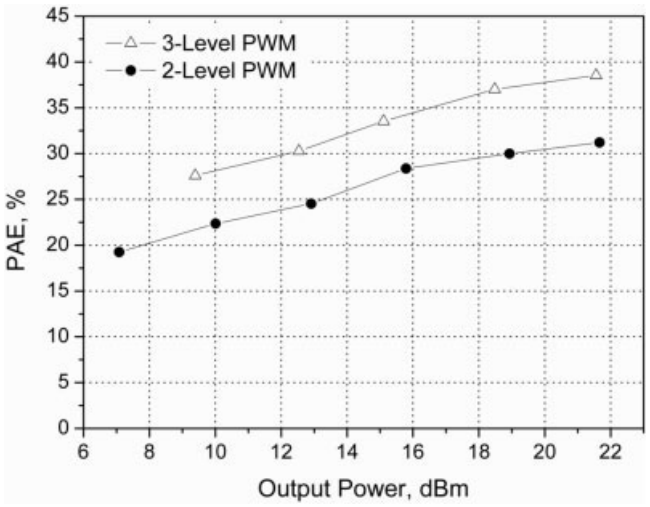

Figure 7 Measured PAE of modulated CDMA signal

duty ratio reduces. When a large PA is being operated, PAE is 50.4% at 27.34 dBm.

4.2. Performance for CDMA Signals

The PWM modulated signal for the CDMA signal is amplified with a switching PA and the measured PAE is 38% at the average power of 22.66 dBm. A three-level PWM modulated CDMA IS-95A signal is applied and the overall efficiency of the transmitter is measured to be 47% PAE, which is 9% higher than conventional PWM. Using a band pass filter, harmonic signals can be removed. To prevent the output signal from distortion due to filtering, an isolator is used. The insertion loss of these components is about 1 dB. The efficiency, including the insertion loss, is reduced to 30.5% and the output power to 21.6 dBm for a two-level PWM, whereas the maximum PAE is 37.6% for three-level PWM at the same power level. If higher sampling frequency and more pulse levels are used, the switching harmonic power will be reduced. Then, it will be possible to remove an isolator and a BPF, which leads to an improvement of the efficiency. Figure 7 shows the PAE measured for the average output power range of 7–22 dBm. These are measured by changing the DC bias conditions and input power to obtain optimum performance. The adjacent channel power ratios (ACPRs) are −42.78 and −54.36 dBc at 885 kHz and 1.98 MHz offset, respectively. The ACPRs meet the specifications of the CDMA IS-95A signal.

5. CONCLUSIONS

A three-level pulse width modulation scheme is presented for improving the efficiency of a linear pulsed power amplifier. An envelope of a CDMA IS-95A signal is modulated by three-level PWM and switches either a lower or a higher power class E power amplifier on and off. After filtering the output pulse signal by the band pass filter, the original signal is restored. The measured overall efficiency is 37.6% at 21.6 dBm output power, while the linearity requirements are satisfied. This shows an improvement of 7.1% of overall efficiency compared with the PA using the conventional PWM scheme.

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CPW-FED ULTRAWIDEBAND SQUARE ANTENNA WITH ROUND CORNERS, A TRIDENT-SHAPED FEEDING STRIP AND SEMIELLIPTIC GROUND

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ABSTRACT: *A novel coplanar waveguide (CPW) fed monopole ultrawideband antenna is proposed to operate from 2.1 to 13.4 GHz. It consists of a square radiator with round corners, a trident-shaped feeding strip, and semielliptic ground. By use of these techniques, the operating bandwidth and radiation performance (approximate omni-directional pattern) can be improved. And then, the relationship between the return loss curves and the geometry of the trident-shaped feeding strip was gotten. Finally, good agreement has been obtained between the simulation and experiment.* © 2009 Wiley Periodicals, Inc. Microwave Opt Technol Lett 51: 1924–1927, 2009; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.24483

Key words: *ultrawideband (UWB); printed monopole antenna; trident-shaped feeding strip*

1. INTRODUCTION

Recently, ultrawideband (UWB) system design and application have become the focus of wireless communications. As an essential part of the UWB system, the UWB antenna has also drawn much attention in recent years [1–8]. The design requirements of the UWB antenna include a broad impedance bandwidths and stable radiation patterns. Many candidates are proposed and analyzed, such as guided-wave radiating structures [3], frequency independent antennas, antennas with structures supporting the TEM wave modes [4], etc. However, compared with the UWB antennas with solid structure, planar antennas have some features, such as low profile, easy to fabricate, and light weight [5–8].

In this article, a novel planar antenna with CPW fed is proposed, it is a evolution from some antennas introduced in literature [3–9]. Especially, Wong et al. [3] have used a trident-shaped feeding strip to widen the bandwidth of planar metal-plated monopole, which has a ground plane perpendicular to the radiator, and so, it is not suitable for integration with a printed circuit board. And finally, based on the advantage of the square plane antenna over other antennas, a CPW-fed square antenna with round corner, a trident-shaped feeding strip, and semielliptic ground is designed and fabricated, which overcomes the disadvantage of the antenna proposed by Wong et al.

2. ANTENNA DESIGN

Figure 1 shows the geometry of the proposed UWB antenna, which consists of a square radiator with round corners, a trident-shaped feeding strip, and a semielliptic ground. The square radiator of 20×20 mm^2 with round corners at four vertexes is used. Radiuses of the four round corners are $R = 5$ mm. Adding four round corner to the square antenna and adopting semielliptic ground change, the current distributions on the ground plane and the radiator which avoid the current change abruptly. Moreover, since the trident-shaped feeding strip has three feeding points symmetrically connected to the lower edge of the radiator, a more uniform current