Low-Power CMOS Super-Regenerative Receiver With a Digitally Self-Quenching Loop

Kihyun Kim, Sumin Yun, Sungho Lee, *Student Member, IEEE*, and Sangwook Nam, *Member, IEEE*

***Abstract*—A 500 MHz super-regenerative receiver (SRR) with a digitally self-quenching loop (DSQL) is designed for low-power/high-data-rate applications. The DSQL replaces the envelope detector used in a conventional SRR and minimizes the overall power consumption by generating a self-quench signal digitally for a super-regenerative oscillator. The receiver is fabricated using a 0.13 μm CMOS process. The chip size is 0.7 mm^2 and the minimum energy usage is 0.09 nJ/b with a supply voltage of 1 V at a data rate of 10 Mbps. The measured sensitivity is -76 dBm.**

***Index Terms*—Capsule endoscopy, digital counter, on-off keying (OOK) modulation, self-quench, super regenerative.**

I. Introduction

In wireless body area networks (WBANs), especially capsule endoscopy systems [1], a transceiver with low power consumption which operates at a high data rate is a key component. A high data rate is required to transmit high-resolution images for accurate diagnoses when using a capsule endoscope. Also, low power consumption is essential when seeking to extend the battery life of the transceiver.

A super-regenerative receiver (SRR) is a suitable receiver structure for short-range wireless communications such as a medical implant communication service (MICS) and, a wireless sensor network (WSN) due to its low power consumption and high gain. Therefore, various types of super-regenerative receivers have been developed for these applications [2]–[8].

To reduce power consumption in a SRR, [4], earlier work [7] used an initial calibration process to set the minimum receiver bias current for the optimum operation. These calibration processes are executed by digital circuits which consume its power only during the initial set-up time of receiver. Other research [6], [8] used quasi-static devices for data acquisition. Quasi-static devices consume power only when they receive an input signal.

In this work, we analyze the SRR proposed in [9] in detail and show the measurement results of the fabricated chip, which operates under a reduced idle current through use of a digitally self-quenching loop (DSQL) with a 2 b digital counter. The DSQL with a zero idle current replaces the envelop detector in the conventional SRR structure and reduces the oscillation time of quench oscillator drastically. Therefore, the power consumption of the receiver is minimized and its efficiency (nJ/b) is maximized. The operating frequency of the SRR is set to 500 MHz for application to a capsule endoscope [10]. The fabricated receiver with a 1 V power supply shows the minimum energy usage of 0.09 nJ/b at 10 Mbps. Its measured sensitivity is -76 dBm with a bit error rate (BER) of 10^{-3}.

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The authors are with the School of Electrical Engineering and Computer Science, Seoul National University, Seoul 151-741, Korea (e-mail: kihyun@ael.snu.ac.kr; ysoom@ael.snu.ac.kr; 2sungho@gmail.com; snam@snu.ac.kr).

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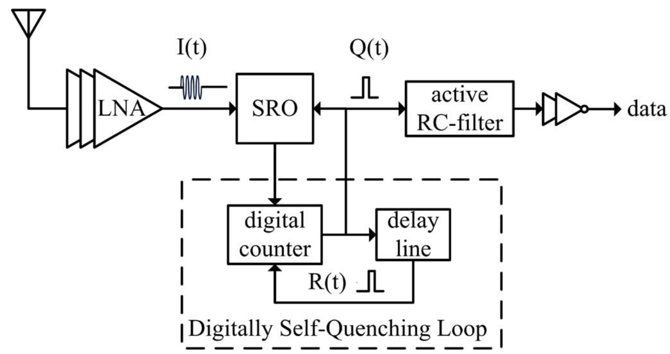

Fig. 1. Block diagram of the proposed receiver.

II. Description of the Receiver

Fig. 1 shows a block diagram of the proposed receiver, consisting of low-noise amplifier (LNA), DSQL, a super regenerative oscillator (SRO), and an active RC-filter with two inverters as the output buffer. The counter in the DSQL counts the number of crests of the SRO output and generates a quench pulse when the counter is full. The reset signal R(t) is a short time-delayed pulse of Q(t), which resets the counter immediately after a quench signal is issued. This process is repeated and the DSQL generates a periodic quench signal Q(t). Therefore, the SRO periodically starts up and shuts off according to the DSQL and the period of the quench signal is dependent on the start-up time of the SRO. When the RF signal I(t) is injected into the SRO by the LNA, the Q(t) period is decreased. The data is recovered by monitoring the dc level at the output of the active RC-filter.

A. Digital Self-Quenching Loop

Fig. 2 shows the gate-level schematic of the DSQL, a simplified version, having a zero idle current during the start-up time of the SRO. A simple 2 b counter is used in the DSQL to minimize its power consumption and to increase the data rate so that it is proportional to the quench rate [11]. The external reset port Rex shown in the figure is adopted to reset the DSQL initially. When the external reset R_{ex} is "1," the quench signal Q(t) expresses "1" to shut off the SRO. R_{ex} is then '0', and all logic

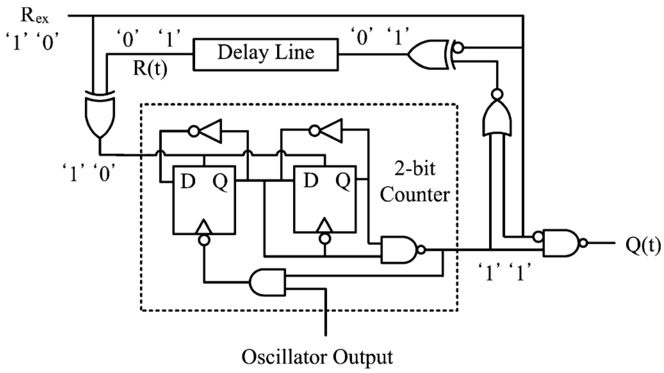

Fig. 2. Gate level schematic of the digital self-quenching loop.

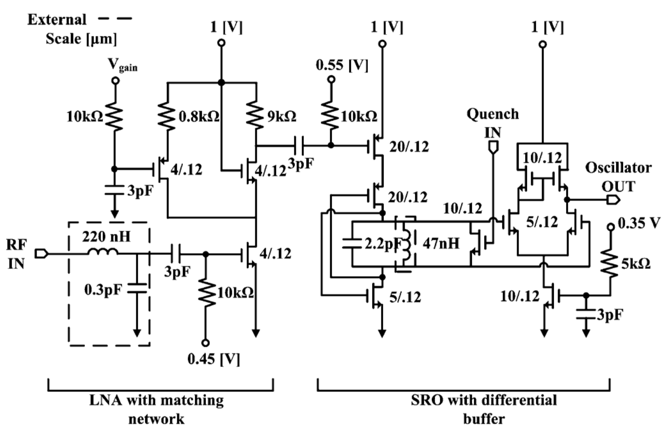

Fig. 3. Schematics of a LNA with a matching network and a SRO with a differential buffer.

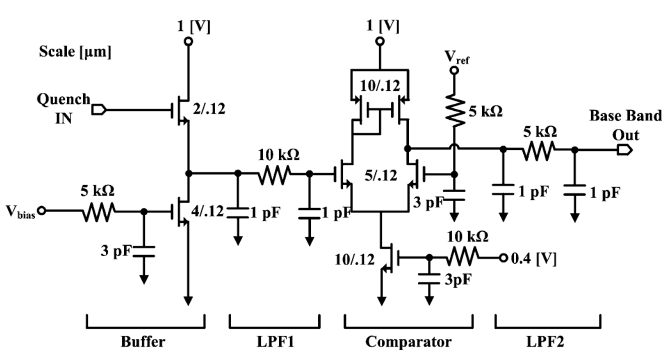

Fig. 4. Schematics of the active RC filter.

gates are operated as buffers and the quench signal Q(t) is fixed at '0.' Next, the SRO starts up and runs, until the binary count number in 2 b counter is "11." When the binary number changes to "11," Q(t) transfers to "1." This inactivates the SRO again. After a time delay, the DSQL is reset by R(t). R(t) is generated by Q(t) through the delay line, which consists of an inverter array. These operations repeat periodically until the DSQL is initialized by an external reset.

B. Design Issues

Fig. 3 shows the schematics of the LNA, and the SRO. The LNA is designed as a three-stage cascade structure to achieve high reverse isolation and gain, although only a single stage

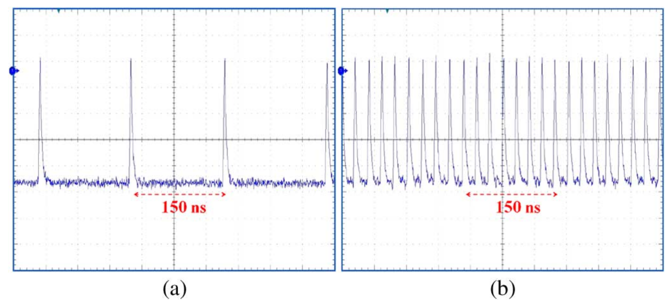

Fig. 5. Measured frequency variation of quench signal Q(t) in time-domain: (a) without RF input signal and (b) with −70 dBm RF input signal.

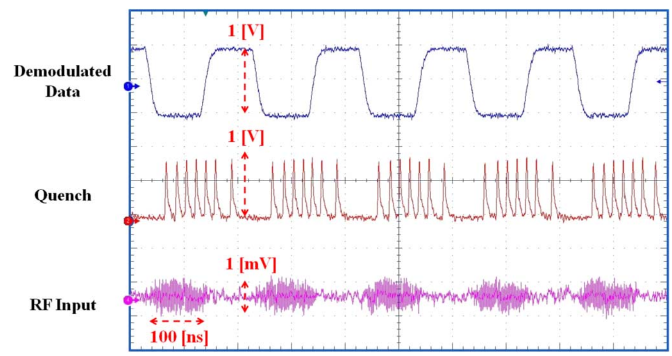

Fig. 6. Measured demodulated data, quench, and RF input signals at 10 Mbps in a time-domain.

is presented in Fig. 3. All stages are identical to the amplifier shown in Fig. 3. The current bleeding technique is adopted to increase the gain by properly biasing V_{gain}. The high gain of LNA is essential for a good sensitivity of proposed receiver. The SRO is a current reuse type which is suitable for low-power and high-speed applications [12]. The SRO is biased near the sub-threshold voltage to maximize the start-up time and minimize its power consumption. A differential buffer is used to connect the digital controller system to the oscillator. The time duration of delay line in Fig. 2 is designed as 5 ns considering a data rate of 10 Mbps and Process Voltage Temperature (PVT) variations. The active RC filter is shown in Fig. 4. The buffer reduces the capacitive loading effect of the DSQL. Also, this structure is suitable for a low-power topology, as the buffer consumes power only when quench signal is "1."

III. Experimental Results

A prototype was fabricated using a 0.13 μm CMOS process according to the block diagram shown in Fig. 1 and Fig. 2. The chip size is 0.7 mm^2 including the pads. The external passive components were used in the matching network of LNA and in the inductor of the oscillator. The measured input bandwidth with −10 dB reference was 8.4 MHz that makes a small degradation of receiver's sensitivity at 10 Mbps.

To verify the DSQL mechanism, the fabricated chip was tested in a time-domain using a Tektronix DPO7254 oscilloscope. When the continuous RF signal with −70 dBm was injected into the receiver, an increased quench frequency [Fig. 5(b)] was generated, which was about seven times higher

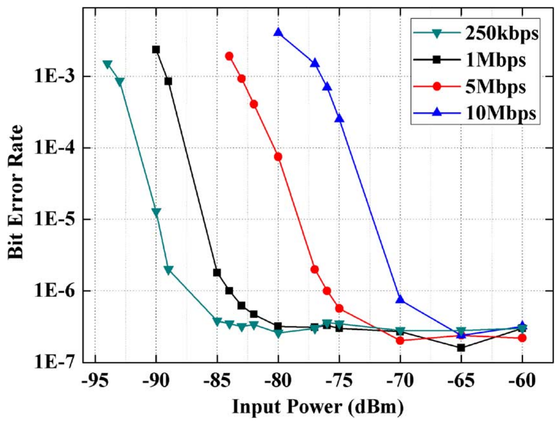

Fig. 7. BER measurement results of the designed receiver.

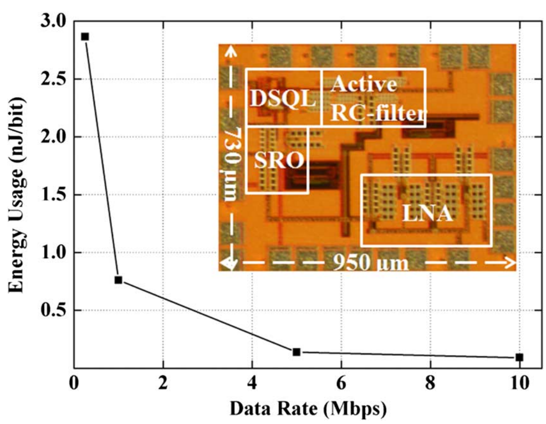

Fig. 8. Total energy consumption for the receiver at each data rates. A chip photo of the proposed receiver is also shown.

TABLE I
COMPARISON WITH A RECENT SUPER-REGENERATIVE RECEIVER

Parameter	[2]	[3]	[7]	[8]	This work
Tech (nm)	180	180	180	180	130
Modulation	FM-UWB	OOK	BFSK	IR-UWB	OOK
Frequency (GHz)	3.5, 4.5	0.402	2.4	3.494, 3.993	0.5
Supply (V)	1.5	1.3	0.65	1.5	1
Power Consumption (mW)	1.5	0.9	0.215	10.8	0.9
Data Rate (Mbps)	2	0.156	2	10	10
Sensitivity (dBm)	*-95	-75	-75	-66	-76
Energy (nJ/bit)	0.75	5.8	0.175	0.24	0.09

* At a BER value of 10^{-6}.

than the original quench frequency [Fig. 5(a)]. Fig. 6 shows the measured signals (demodulated data, quench, RF input) when the on-off keying (OOK) signal with 10 Mbps came to the receiver. The result shows that the number of quench cycles generated per received symbol is seven.

The BER of the fabricated chip was measured using an Agilent E4438C signal generator. For this measurement, a PN23 random OOK signal with a total 10 Mb was used. The V_{bias} value in the active RC filter was fixed at 0.3 V, while the V_{ref} value was properly biased externally. The measurement results for different data rates (250 kbps. 1 Mbps, 5 Mbps, 10 Mbps) are presented in Fig. 7. The sensitivity levels with BER values of 10^{-3} were -93 dBm, -89 dBm, -83 dBm, -76 dBm, respectively. Fig. 8 shows the total energy consumption for the receiver at each data rate. The minimum energy usage is 0.09 nJ/b at 10 Mbps.

Table I shows a comparison of the proposed receiver and SRRs described in a recent publications [2], [3], [7], [8]. The results show the low-power/high-data-rate characteristics of the proposed receiver.

IV. CONCLUSION

In this letter, we propose a new type of SRR which uses a DSQL for low-power/high-data-rate applications. The designed receiver with the DSQL exhibits good sensitivity (-76 dBm), low energy usage (0.09 nJ/b at 10 Mbps) and simplicity without an envelop detector. The experimental results show that the proposed structure is suitable for low-power medical implant applications or capsule endoscopy applications which require a high data rate.

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