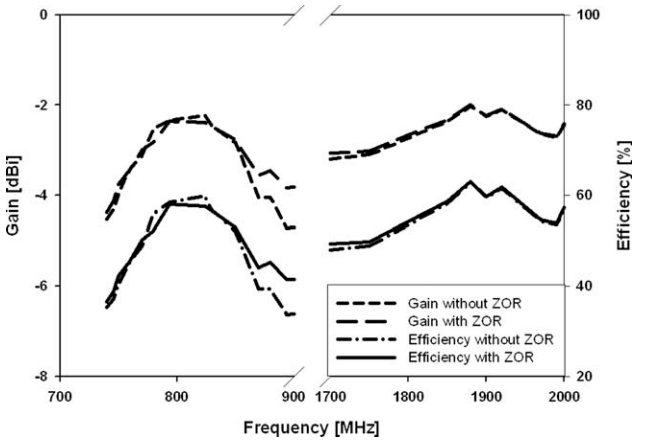


**Figure 5** Comparison of measured antenna gain and efficiency with and without ZOR. - - -, Gain without ZOR; – –, gain with ZOR; - · -, efficiency without ZOR; and —, efficiency with ZOR

In this article, an internal, compact, multiband antenna for an USB dongle application is proposed. The designed antenna simultaneously satisfied the voltage standing wave ratio (VSWR) by less than 2:1 for the following applications and their respective frequency range bands: long-term evolution (LTE), range of 746 to 794 MHz; digital cellular network (DCN), range of 824 to 894 MHz; and personal communication system (PCS)-1900, range of 1850 to 1990 MHz.

## 2. ANTENNA DESIGN

The geometrical configuration of the proposed antenna is shown in Figure 1. A folded inverted-L (IL) antenna, 30 ×15 × 7 $mm^3$, is constructed on a plastic carrier with a relative-dielectric constant of 3.2 and is located at the top edge of the ground. The size of the system ground plane is 30 × 52 $mm^2$, a common dimension for a general USB dongle, and is installed on FR4 substrate ($\varepsilon_r = 4.4$) as shown in Figure 1(a). The IL antenna illustrated in Figure 1(c) is primarily composed of two-pronged elements. The IL-shaped zeroth-order resonator (ZOR), which is located near the feed point, is introduced on the backside of the substrate as shown in Figure 1(b). The ZOR makes use of the opposite-phase property of right-handed and left-handed (LH) transmission lines, which has been proven experimentally. Because LH transmission lines do not exist in nature, an artificial lumped element is used. A LH transmission line consists of a series capacitor ($C_L$) and a shunt inductor ($L_L$) as shown in Figure 1(d). The gap between the feed and ZOR provides the required LH series $C_L$ in Figure 1(a), and the lumped element inductor introduces LH shunt $L_L$ in Figure 1(b).

To observe the effect of the ZOR, the simulated VSWR characteristics with and without a ZOR, are compared in Figure 2. The dual resonances near 800 and 2000 MHz are generated by two-pronged IL antenna elements. The lengths of the two asymmetric arms provide tuning capability for both low and high frequencies. Adding the ZOR on the backside of the substrate greatly enhanced the impedance bandwidth that was achieved for the DCN bandwidth.

The length and width of the antenna are determined by using a commercial design tool, CST Microwave Studio [5].

## 3. RESULTS

Figure 3 shows the measured VSWR characteristics of the proposed antenna. It is shown that the designed antenna simultaneously satisfied the VSWR of less than 2:1 for LTE, DCN, and PCS-1900 frequency bands. Figures 4(a)–(d) depict the three-dimensional (3D) radiation patterns of the designed antenna at 760, 870, 1880, and 1970 MHz, respectively. To accommodate practical use, the proposed antenna is to be embedded in the left side of a laptop computer. Figure 5 shows the measured antenna gain and efficiency with respect to frequency. Gains are shown as short- and long-dash lines, and the efficiency is illustrated as dash-dot and solid lines in Figure 5. The measured antenna efficiency result shows that the ZOR can provide over a 10% improvement for the DCN frequency band. The average antenna gain varies from approximately −4.38 to −2.09 dBi across the entire bandwidth.

## 4. CONCLUSION

A compact, internal, IL antenna with a ZOR is proposed. The designed antenna has a simple structure and is straightforward to fabricate. The wide impedance bandwidth in the lower band is obtained by adding a ZOR structure. The proposed antenna is a superior choice for use in multiband wireless applications, due to its ability to satisfy USB dongle terminal size constraints and to provide a wide impedance bandwidth.

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# AN EFFICIENT CMOS POWER-COMBINING TECHNIQUE WITH DIFFERENTIAL AND SINGLE-ENDED POWER AMPLIFIER

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**ABSTRACT:** *This article proposes an efficient power-combining architecture with differential and single-ended power amplifiers (PAs) in a CMOS process. The single-ended amplifier is added for overall efficiency enhancement. To demonstrate this concept, a CMOS PA using the proposed architecture was fabricated with a 0.13-μm CMOS technology that delivers 30.6 dBm of output power with 42% drain efficiency and 38% power-added efficiency at 1.95 GHz.* © 2010 Wiley Periodicals, Inc. Microwave Opt Technol Lett 52:2214–2217, 2010; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.25460

**Key words:** *CMOS; power combiner; transformer; impedance transformation; power amplifier*

## 1. INTRODUCTION

CMOS power amplifiers (PAs) have attracted a great deal of attention in recent years. The integration of radio frequency (RF) components including PA is essential for realizing the true meaning of system-on-a-chip. In addition, PA is the most important component used to determine overall RF transmitter efficiency because it consumes the largest portion of DC power.

However, several factors deteriorate the performance of CMOS PAs. First, the low breakdown voltage of the transistor limits the output power. To overcome this problem, various combining approaches have been developed, such as the series stack method [1] and the transmission line–based combiner [2]. Among them, a distributed active transformer (DAT) efficiently achieves a high output power and impedance transformation [3, 4]. Second, highly conductive substrates and thin metal layers reduce efficiency of on-chip passive devices. In spite of lossy on-chip passive characteristics, a transformer is a crucial component for implementing the power-combining architecture.

For these reasons, a watt-level CMOS PA using an on-chip power combiner delivers output power with relatively low efficiency. In this article, a conventional power-combining method and the problem associated with CMOS PAs are briefly described. Then, an efficient power-combining method that alleviates the effects of lossy transformers is proposed and analyzed.

## 2. MULTILEVEL DIGITAL PULSE MODULATION

### *2.1. Conventional DAT*

The simplified architecture of DATs is shown in Figure 1. It uses several 1:1 transformers to combine power. In this architecture, the identical AC voltage sources are arranged in series on the secondary part. Therefore, $R_{PA}$ and the output power at the output terminal are related to the number of power stages. They can be calculated as

$$V_{OUT} = K \cdot V$$
$$R_L = \frac{K \cdot V}{I_S}$$
$$R_{PA} = \frac{V}{I_S} = \frac{R_L}{K} \quad (1)$$
$$P_{OUT} = K \cdot \frac{V_{DD}^2}{R_{PA}}. \quad (2)$$

As shown in (2), the output power is $K$ times higher than one PA using an ideal 1:1 transformer. Thus, this concept is one efficient power-combining method for a CMOS PA with a watt-level output power. However, a shortcoming of this architecture is the low passive efficiency of each transformer. Actually, the maximum available gain (MAG) of the transformer is less than $-1.3$ dB [5]. This can significantly degrade the performance.

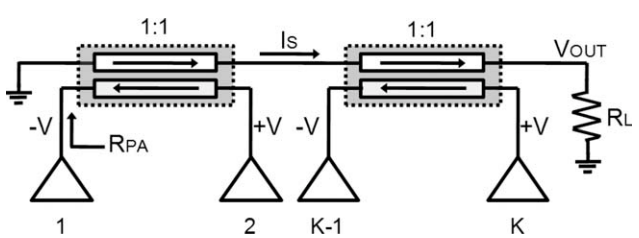


**Figure 1** Conventional distributed active transformer

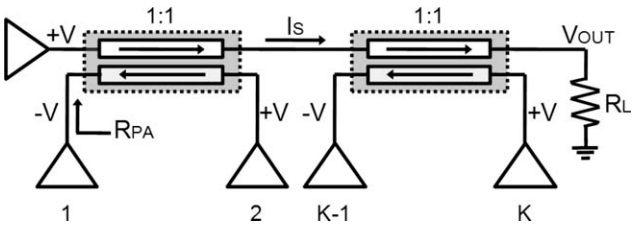


**Figure 2** The proposed architecture using an additional single-ended power amplifier

### *2.2. Proposed Architecture*

Figure 2 shows the new efficient power-combining architecture with differential and single-ended PAs. The role of single-ended PA is to increase a portion of lossless power at the output. In the conventional architecture, the AC voltage sources suffering from a transforming loss are arranged in series. In the proposed architecture, one of them operates as a lossless voltage source due to the additional single-ended PA. This concept can maximally enhance overall power efficiency. If PAs consider ideal voltage sources, a simplified analysis of the circuit is similar to that of the conventional DAT.

$$V_{OUT} = (K+1) \cdot V \quad (3)$$
$$R_{PA} = \frac{V}{I_S} = \frac{R_L}{K+1} \quad (4)$$

Figure 3 shows efficiency enhancement due to the additional single-ended PA. In the case of lossy transformers, the proposed architecture presents greater enhanced efficiency than does the conventional architecture. In addition, as illustrated in Figure 3, better performance is exhibited when the minimum number of differential PAs is used. Consequently, we can conclude that the value of $K$ is 2 for the large portion of lossless power at the output.

## 3. ANALYSIS OF PROPOSED METHOD

As seen in (4), with the assumption of an ideal voltage source, $R_L$ is divided by the number of PAs similar to Eq. (1). However, no PA operates as a perfect voltage source. Thus, an analysis

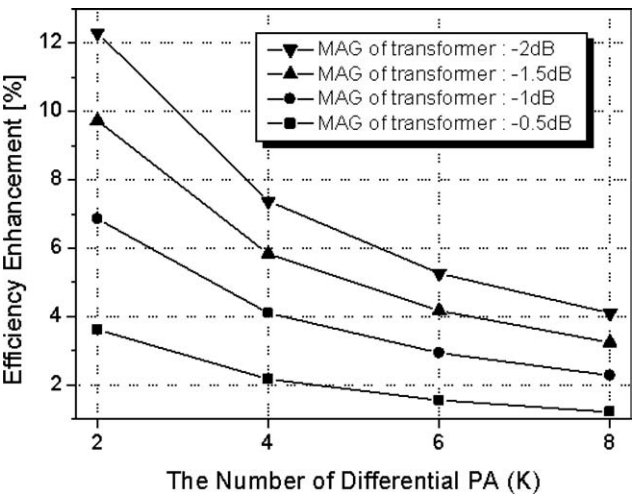


**Figure 3** Efficiency enhancement due to additional single-ended PA versus the number of differential PA for different MAG of transformers

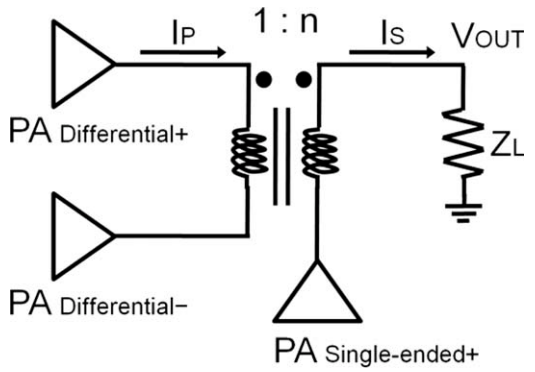


**Figure 4** The simplified circuit of the proposed architecture

including source impedance of PAs is needed, because that of single-ended PA on the secondary path may cause asymmetry in each RPA.

Figure 4 shows the simplified circuit of the proposed architecture, where $K$ of the circuit shown in Figure 2 is 2 and a turn ratio of the transformer is 1:$n$. Figures 5(a) and 5(b) show the equivalent model for the transformer of Figure 4, as seen in the active devices. The impedance seen by the differential PA calculated as the ratio between the current of the primary path and the output voltage of the PA can be derived as follows:

$$I_{\mathrm{P}} = \frac{2V + \frac{V}{n}}{2Z_{\mathrm{S}} + \frac{Z_{\mathrm{L}} + Z_{\mathrm{S}}}{n^2}}$$
$$Z_{\mathrm{PA1}} = \frac{V - I_{\mathrm{P}} \cdot Z_{\mathrm{S}}}{I_{\mathrm{P}}} = \frac{2Z_{\mathrm{S}} + \frac{Z_{\mathrm{L}} + Z_{\mathrm{S}}}{n^2}}{2 + \frac{1}{n}} - Z_{\mathrm{S}} \tag{5}$$

Based on these conditions, $Z_{\mathrm{PA1}}$ is computed as a function of not only $Z_{\mathrm{L}}$ but also $Z_{\mathrm{S}}$. However, where $n$ is unity, $Z_{\mathrm{PA1}}$ is not affected by source impedance $Z_{\mathrm{S}}$.

$$Z_{\mathrm{PA1}} = \frac{Z_{\mathrm{L}}}{3} \tag{6}$$

A similar approach is used for the analysis of the secondary path case in Figure 5(b), as follows:

$$Z_{\mathrm{PA2}} = \frac{Z_{\mathrm{S}} + 2Z_{\mathrm{S}} \cdot n^2 + Z_{\mathrm{L}}}{1 + 2 \cdot n} - Z_{\mathrm{S}} \tag{7}$$

In addition, if it is assumed that $n$ is 1 in Eq. (7), the impedance seen by the single-ended PA and load impedance relation is

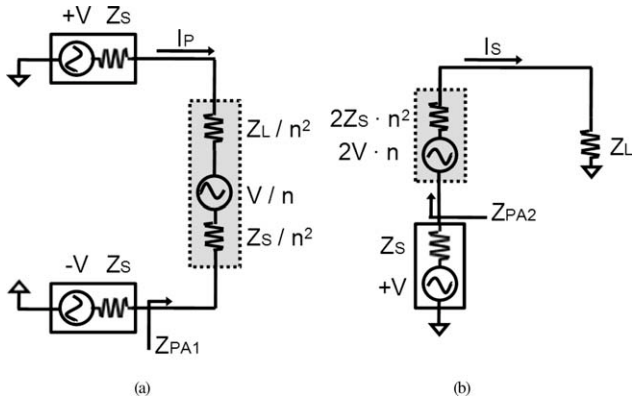


**Figure 5** (a) Network for calculating impedance seen by the differential PA. (b) Network for calculating impedance seen by the single-ended PA

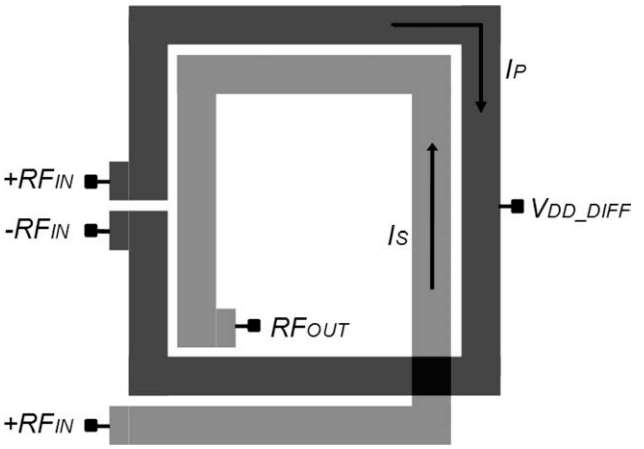


**Figure 6** Layout of the proposed power-combining transformer

$$Z_{\mathrm{PA2}} = \frac{Z_L}{3} \tag{8}$$

In summary, the proposed architecture has characteristics for impedance transformation similar to those of conventional DAT, where the additional reasonable design criterion is that transformers have a 1:1 transform ratio.

## 4. POWER-COMBINER DESIGN

Generally, the standard CMOS process is not considered as a good candidate for on-chip passive devices [6, 7]. To meet many demands of output networks for PAs, metal traces with wide widths such as ''power inductors,'' [8] are tied to implement low loss passives. In this design, a standard 0.13-$\mu$m CMOS process with eight metal layers is used. This process provides the top metal of 2-$\mu$m thickness for on-chip passive elements. There are specific design guidelines for drawing the layout of the proposed structure. First, the lengths of the primary and secondary winding are identical for 1:1 transform ratio. Second, because of high DC currents, the metal width of the transformer is wide enough to avoid electromigration problems. Finally, circular geometry is used for utilizing almost all currents of the primary path, IP.

The width and spacing of the metal traces is 45 and 3 $\mu$m, respectively, and are optimized between the parasitic resistance and substrate loss. The MAG of the designed transformer is simulated as approximately $-1.4$ dB at the frequency of interest.

## 5. EXPERIMENTAL RESULTS

The proposed power-combining architecture for CMOS PA, including the driver stage and input balun, was fabricated using the 0.13-$\mu$m standard CMOS process. For high efficiency, a topology of the class-E switching PA [9, 10] was used in the power stage. The chip photograph is shown in Figure 7. The chip area is $1.5 \times 1.2$ mm$^2$ including the transformers and the bonding pads. The losses of the bond wires, input transformer, and printed circuit board interconnections are included in the PAs measured performance.

The measured and simulated power-added efficiency (PAE) versus supply voltage VDD are plotted in Figure 8 along with output power at 1.95 GHz. VDD varies from 1.2 to 3.3 V, while other factors remained constant during the sweep. The amplifier achieved a PAE of 38% at a maximum output power of 30.6 dBm. Figure 9 shows the measured drain efficiency (DE), PAE,

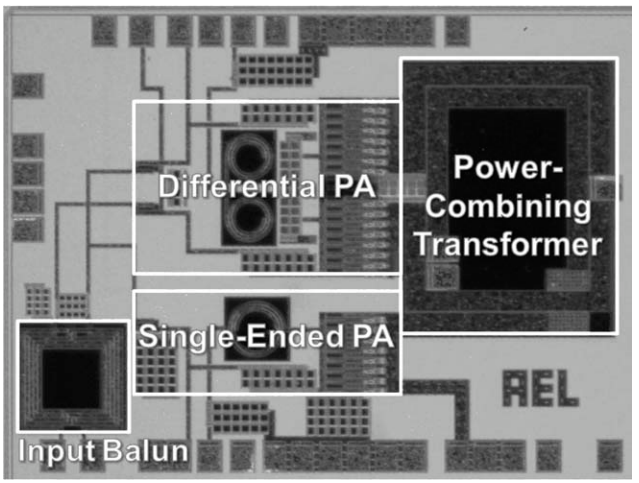


**Figure 7** Chip photograph of proposed CMOS PA

and output power according to operating frequency with a 3.3-V supply voltage of the power stage. The maximum DE and PAE were measured as 42 and 38%, respectively, at 1.95 GHz. The flatness of the output power is 1 dB at worst for an operating frequency between 1.85 and 2.05 GHz. The second harmonic is −43.2 dBc and the third harmonic is −43.7 dBc. These measured results show the comparable PAE for on-chip combining CMOS PAs published thus far [4, 5, 11, 12]; however, these measured results present slightly degraded performance in comparison with the simulated results. We contend that the impedances seen by amplifiers, $Z_{PA1}$ and $Z_{PA2}$, are not identical due to asymmetric parasitic effects of the transformer. Thus, extra design considerations for a symmetric transformer are needed to obtain better performance.

## 6. CONCLUSIONS

In this article, a new power-combining architecture using differential and single-ended PAs has been proposed. The additional single-ended PA performs as a lossless power source. The analysis shows this structure provides an efficient impedance transformation. To demonstrate this concept, a 1.95-GHz CMOS PA was implemented with a 0.13-$\mu$m standard CMOS process. The amplifier achieved a PAE of 38% at a maximum output power of 30.6 dBm.

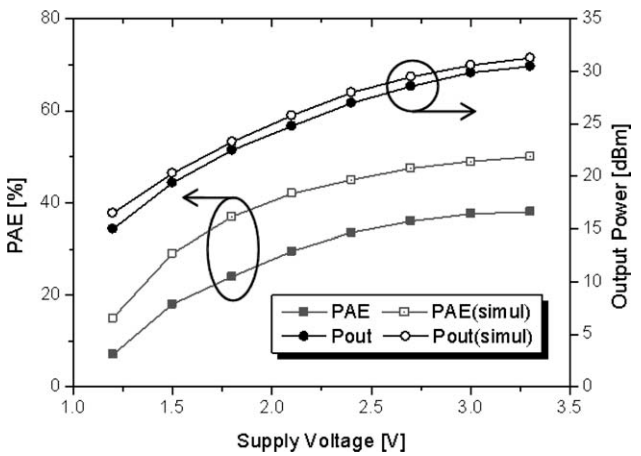


**Figure 8** Measured and simulated PAE and output power versus supply voltage

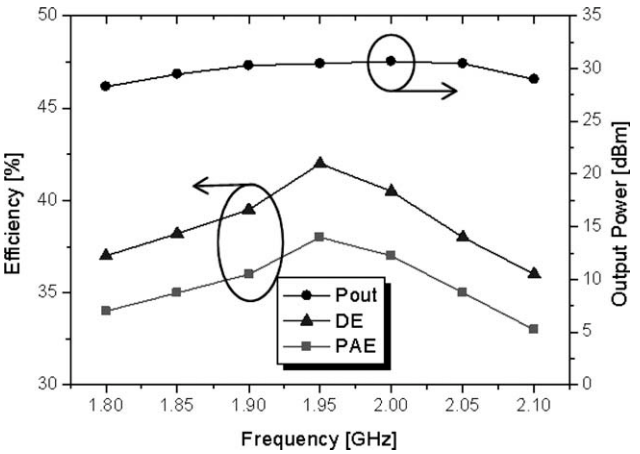


**Figure 9** Measured PAE, DE, and output power versus operating frequency


## ACKNOWLEDGMENTS

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