Self-Calibrated Two-Point Delta–Sigma Modulation Technique for RF Transmitters

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***Abstract*—A self-calibrated two-point delta–sigma modulation technique for CMOS RF transmitter is proposed. This calibration technique employs voltage-controlled oscillator (VCO) and delta–sigma modulator input ports in a frequency synthesizer. By monitoring the control voltage of a loop filter, the gain mismatch between two paths can be detected and completely calibrated by modifying the gain of the VCO path. The acceptable timing mismatch between the two paths is also investigated so that the timing can be controlled to ensure stable output performance. As a result, the phase modulation guarantees a robust performance against PVT variations without using any predistortion techniques. This technique is applied to a quad-band (850/900/1800/1900) GSM/EDGE transmitter for verification. For the amplitude modulation of the EDGE mode, a dc calibration is adopted to suppress unwanted carrier leakage tones. The measurement results show satisfactory GSM/EDGE spectrums and error vector magnitude performance at both low- and high-frequency bands.**

***Index Terms*—CMOS, delta–sigma modulation, EDGE, GSM, polar loop, transmitter, two-point modulation.**

I. Introduction

With the increasing use of multiband/multimode wireless equipment, cost/size-effective design becomes one of the major design goals for mobile devices.

Previous work on RF transmitters have proposed several architectures; mainly, super-heterodyne, direct upconversion, and polar modulation have been employed [1]–[5]. Among them, the polar modulation type has been widely used in the RF transmitter for a nonconstant envelope-signal because the separate process of the amplitude and the phase signal could be effective. In this polar modulation, the phase signal is upconverted with the RF carrier signal by several methods: offset phase-locked loop (OPLL), one-point delta–sigma modulation, and two-point modulation [5]–[16].

Among these structures, the two-point modulation technique circumvents the limited phase-locked loop (PLL) bandwidth problem by splitting the modulated signal into two portions and sending one portion to the voltage-controlled oscillator (VCO) input and the other to the delta–sigma modulator. Although one-point modulation can also be implemented with the calibrated VCO gain and the pole location, the two-point modulation technique is preferred to process multiband or wideband signals [16]. This two-point modulation technique results in constant modulation sensitivity regardless of the loop bandwidth. The strict relation between the PLL bandwidth and modulation bandwidth can be alleviated; thus, the loop bandwidth can be decided for other requirements, such as a narrow PLL bandwidth for low out-of-band noise. In addition, RF circuitry using two-point modulation can be implemented at low cost and with high integration. This method can easily provide multiband/multimode functionality. Therefore, this modulation technique provides a promising solution for various wireless applications that support a wide bandwidth and various frequency bands. However, in the two-point modulation, the timing and the gain matchings between two modulation paths are challenging issues to prevent signal distortions. In order to resolve these problems, accurate timing control and gain matching should be achieved under process and temperature variations conditions. In addition, the design of the VCO control port is crucial to performance, because the dynamic range and linearity at the VCO control port affect the modulated signal quality.

Although the all-digital PLL showed full integration with a satisfying performance, it still suffers from the limited tracking range and its complicated design procedure. Moreover, both the time resolution of the time-to-digital converter and the digital-controlled oscillator gain are sensitive PVT parameters since they are related to the minimum inverter delay and affected by the nonlinear varactor gain, respectively [9]–[12].

There have been a few two-point modulation solutions using the widely used analog PLL. [13] and [14] showed the phase-noise monitoring method at the output of a VCO and manual calibration based on an open-loop design. The work in [15] showed the calibration technique of modulating path gain using a non-ideal bias voltage during a limited time. This technique cannot completely calibrate nonlinear gain during a normal operation due to the disturbances to the bias voltage and nonlinear varactor gain. Therefore, those techniques do not guarantee robust

Manuscript received August 28, 2009; revised February 27, 2010 and April 01, 2010; accepted April 05, 2010. Date of publication June 07, 2010; date of current version July 14, 2010. This work was supported by the Korea Science and Engineering Foundation through the National Research Laboratory Program funded by the Ministry of Science and Technology under Contract ROA-2007-000-20118-0(2007).

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Digital Object Identifier 10.1109/TMTT.2010.2049693

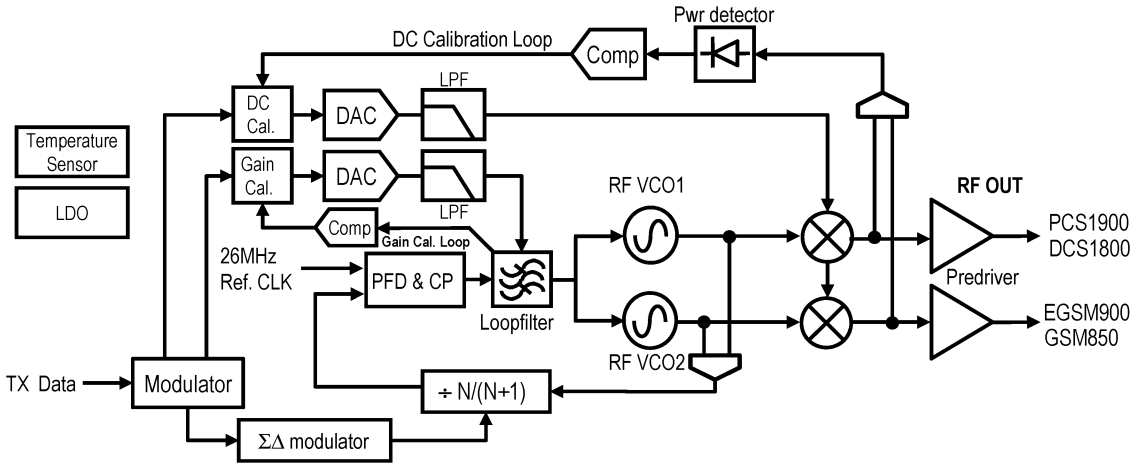


Fig. 1. Block diagram of GSM/EDGE transmitter using the proposed two-point modulation.

design because the gain nonlinearity and timing mismatch can be largely dependent on the PVT variations.

In this paper, we propose a two-point modulation technique using closed-loop self-calibration. This proposed technique achieves wideband phase modulation with robust performance. In addition, a dc calibration is used for amplitude modulation. This calibration technique is applied to a quad-band GSM/EDGE CMOS transmitter, thereby solving timing, gain, and dc problems. Section II gives a brief review of the transmitter architecture, focusing on the two-point modulation loop. Section III describes the proposed self-calibration techniques applied in the transmitter. Finally, Sections IV and V give the measured results and conclusion, respectively.

II. System Architecture Description

Fig. 1 presents the block diagram of an RF transmitter using the proposed two-point modulation. The transmitter utilizes a polar loop architecture that consists of phase modulation using two-point modulation and amplitude modulation using a mixer. The predriver is designed to generate a maximum output power of 3 dBm for driving an external conventional power amplifier (PA). The open-loop-type polar architecture has the advantage of a simple combination of phase modulation with supporting amplitude modulation. Therefore, we used the open-loop type of polar architecture using a gain amplifier. The amplitude modulation operates only in the polar loop mode. In the transmitter, one PLL with two VCOs is used to cover the two frequency bands.

The input ports of both the delta–sigma modulator and the VCO in the fractional-N PLL are utilized as the injection points for two-point modulation. A phase-modulated baseband signal is added to the 22-bit fractional data in the input of the delta–sigma modulator in digital form. For the input path of the VCO, an additional varactor is used for injecting the modulated signal that comes from a 10-bit current-steering digital-to-analog converter (DAC) and a low-pass filter. The analog low-pass filter eliminates unwanted spurious frequency tones from the DAC output signal. For phase modulation, gain and timing mismatches are eliminated by the proposed calibration techniques. By monitoring the variation patterns of the control voltage of the loop filter in the PLL, the gain mismatch is detected and estimated. The measured voltage patterns are compared with the original signal, and then the gain mismatch is eliminated by the amplitude scaling included in the digital logic. The calibrated transmit data flow to the VCO via the 10-bit DAC. For amplitude modulation, the phase and magnitude mismatches of the local oscillator (LO) signal are measured by a feedback loop. As a result, the feedback loop minimizes carrier leakage by removing the dc tone. In Section III, the gain, timing, and dc calibration techniques will be explained in more detail.

III. Proposed Self-Calibrated Transmitter

A. Analysis of Two-Point Modulation Technique

Fig. 2 shows a model of the transmitter using two-point modulation. Although jitter noises from the charge pump, VCO, and reference signal exist, they were assumed to be negligible in this analysis since the injected modulated signal is generally much larger than the jitter noises. τ_1, τ_2, K_1, and K_2 represent, respectively, the timing delays of the two signal paths and the frequency gains of the modulated signal paths. The PLL parameters include the VCO frequency gain (K_v) and the combined gain (K_d) of the phase-frequency detector and the charge pump. For simple analysis, although the third-order loop filter is actually used in the PLL, the transfer function of the loop filter $F(s)$ was simply modeled as a the first-order loop filter by $F(s) = (1 + sa)/sb$, where a and b represent the resistive and capacitive time constants, respectively. This assumption is valid because the loop filter order does not affect the interaction between the two-point modulated signal and the PLL characteristics. The loop filter order can just affect the magnitude of the effect of the modulated signal, which will be shown in the relation of loop filter voltage and modulation signal. The divider modulus is equal to N. The transmit signal phase is represented by $\phi_{\rm sig}$. When it is assumed that the reference signal phase $\phi_{\rm ref}$ is zero, the relation between output signal phase $\phi_{\rm out}$ and $\phi_{\rm sig}$ is formulated as

$$\phi_{\rm out} = H_m(s) \cdot V_{\rm sig} \tag{1}$$

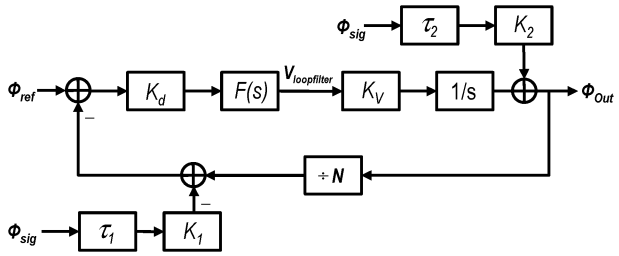


Fig. 2. PLL model with two-point modulation.

where

$$H_m(s)=\frac{e^{-s\tau_1}\cdot N\cdot K_1\cdot K_d\cdot K_v\cdot F(s)+e^{-s\tau_2}\cdot K_2\cdot N\cdot s}{s\cdot(N\cdot s+K_d\cdot K_v\cdot F(s))} \tag{2}$$

$$\phi_{\rm sig}=\frac{K_{\rm sig}}{s}\cdot V_{\rm sig} \tag{3}$$

$$\frac{\phi_{\rm out}}{\phi_{\rm sig}}=\frac{b\cdot e^{-s\tau_2}\cdot K_2\cdot N\cdot s^2+e^{-s\tau_1}\cdot N\cdot K_1\cdot K_d\cdot K_v\cdot(a\cdot s+1)}{K_{\rm sig}\cdot(b\cdot N\cdot s^2+K_d\cdot K_v\cdot(a\cdot s+1))} \tag{4}$$

where $K_{\rm sig}$ represents a nominal frequency gain of the modulated signal. In (4), as the frequency approaches 0, the final value approaches $NK_1e^{-s\tau_1}/K_{\rm sig}$. In reverse, as the frequency approaches infinity, the value of the combined magnitude function becomes $K_2e^{-s\tau_2}/K_{\rm sig}$. To achieve a uniform frequency response, the condition can be manipulated as follows:

$$e^{-s\tau_1}\cdot N\cdot K_1=e^{-s\tau_2}\cdot K_2. \tag{5}$$

Therefore, to achieve a balance of the two-point modulation, the timing and gain matches at the two points should be related as follows:

$$K_2=N\cdot K_1 \quad \tau_1=\tau_2. \tag{6}$$

Equation (6) indicates that the timing and gain matching should be guaranteed at the same time. As for the behavioral simulation with the GMSK signal, the error vector magnitude (EVM) performances with timing and gain mismatches are shown in Fig. 3(a) and (b). According to the simulation, the allowable timing mismatch should be under one clock cycle to secure the spectrum mask and EVM performance. One clock cycle corresponds to 1/26 MHz. In addition, the required gain mismatch should be below 1%. In the simulation, the minimum EVM is limited to 0.7% under the conditions of perfect gain and timing matches because the DAC quantization noise and the nonlinearity of the variable gain amplifier (VGA)/mixer and the output preamplifier are considered. Although the rms EVM specification of EDGE is 9% at PA, the design target rms EVM was set to 3% at the preamplifier output.

Fig. 4 shows the transmitter structure using two-point modulation. Because the data injection in the delta–sigma modulator gives us the freedom to accurately control timing with digital processing, the channel information and the modulating signal are summed at this modulator input port. For the high-pass filter characteristic, a varactor modulates the transmit signal at the VCO. To convert the digital signal to analog data, a low-pass filter eliminates the harmonics of the clocking frequency in

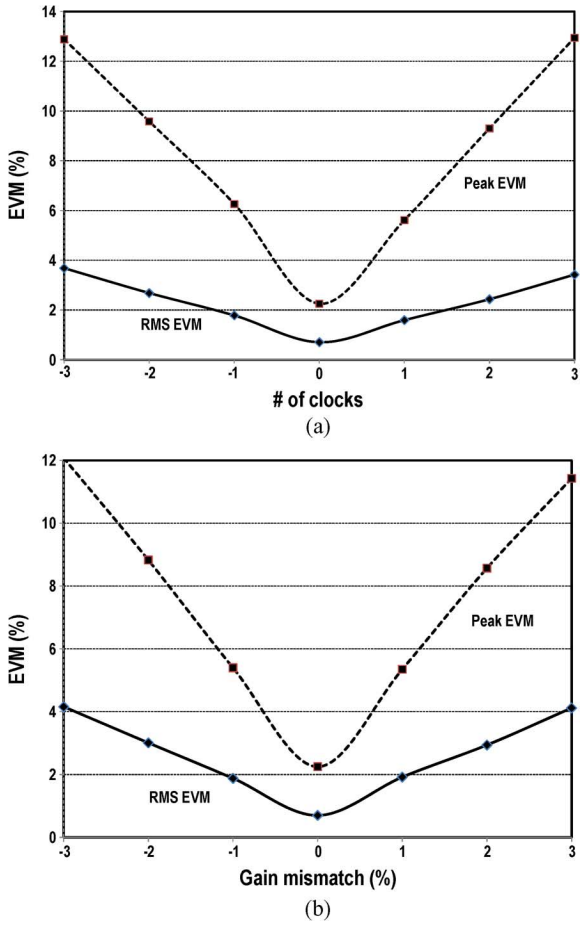


Fig. 3. Mismatch effects on EVM performance. (a) Timing mismatch. (b) Gain mismatch.

the output of the DAC. For the resolution of the DAC, a 10-bit DAC is adopted to guarantee a sufficient EVM performance margin. After the low-pass filtering, a differential-to-single (diff-to-single) buffer converts the differential signals of the low-pass filter using the output range that provides flat frequency gain at the varactor.

Before gain matching, the timing delays over two modulating paths are investigated for the timing matching. The signal paths A1 and A2 are to measure gain mismatch. The signal paths B1 and B2 are the two injected modulating signal paths. Thus, the path delays of A1 and A2 should be the same. Also, the path delays of B1 and B2 should be the same. Some blocks, such as the ac coupler, low-pass filter, diff-to-single converter, and loop filter, have frequency-dependent characteristics, thus these blocks are simulated at PVT variations. Then, similar models are developed using digital logics ($\rm FIL_{Emul}$). In addition, tunable digital delay blocks ($\rm DLY_{Cal}$, $\rm DLY_{Phase}$, and $\rm DLY_{Mod}$) are utilized to adjust the path delays. The timing analysis is conducted with both the dedicated analog delay models and digital blocks using a clocking interval. From Fig. 3(a), 2% rms EVM performance is guaranteed under the conditions of the worst 40-ns delay mismatch. According to the operating temperature, the digital delay block is designed to simply control the delay. The delay compensation can be conducted often using

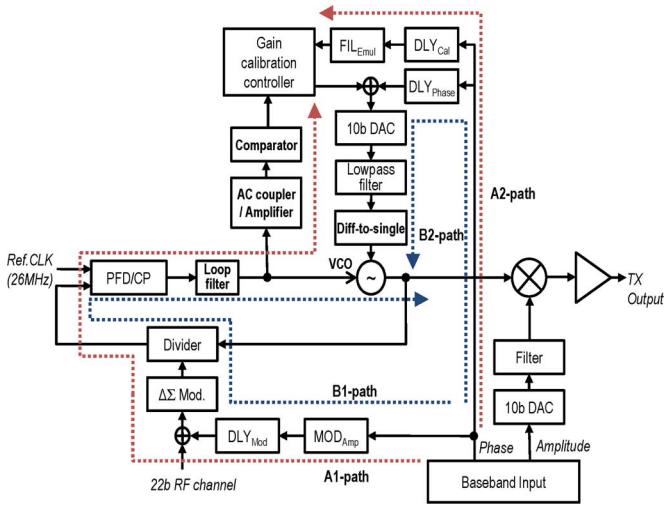


Fig. 4. Two-point modulation transmitter structure.

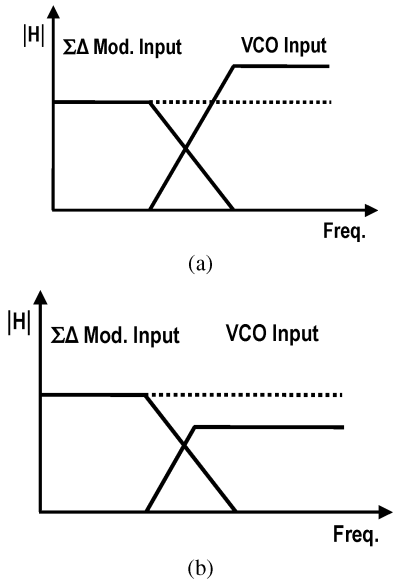


Fig. 5. Transfer curves at the output according to gain variations: (a) too-large gain in the VCO path and (b) too-small gain in the VCO path.

a map-table with temperature settings during the power-on period and guard-time using internal temperature sensor. The map table consists of digital delay settings according to several temperatures. The digital output of the temperature sensor is proportional to the temperature in 10-degree steps. The digital delay is selected with predefined values of the map table. The optimum values of the map table can be chosen by EVM measurements to cover the temperature variation. With this delay compensation, a stable timing margin over the PVT corners can be achieved.

B. Gain Mismatch Calibration

Because the varactor gain for modulating at the VCO is nonlinear, the gain mismatch cannot be compensated for by the method used for the timing mismatch. Moreover, the gain characteristics vary considerably according to the operating frequency, temperature, and process variation. The gain also depends on the resolution of the DAC in front of the varactor. Therefore, gain calibration should be required to compensate for the variations. Since the modulating gain at the delta–sigma modulator path always shows the constant value in digital form, the basis of the calibration will be the gain at the path of the delta–sigma modulator. According to the modulating gain variation at the VCO injection path, Fig. 5(a) and (b) shows the transfer curves of the PLL output. Using superposition with the lowpass and high-pass transfer curves characteristic, frequency-independent data transmission can be achieved. When this gain is larger or smaller than that at the path of the delta–sigma modulator, the frequency response severely deteriorates the transmit data.

The gain calibration starts with measuring the voltage change of the loop filter. The output voltage of the loop filter in the PLL should be constant after the PLL locking except for the effect of the quantization noise from the delta–sigma modulator. Generally, the quantization noise is much less than that of the injected signal. When the only existing gain mismatch is between the injection ports of the two-point modulation from (1)–(3), the relationship between the loop filter voltage and the injected signal voltage can be expressed as follows:

$$\frac{V_{\text{loopfilter}}}{V_{\text{sig}}} = \frac{e^{-s\tau} \cdot (N \cdot K_1 - K_2)}{K_v + \frac{N \cdot s}{K_d \cdot F(s)}} \tag{7}$$

where the timing delays are the same $(\tau = \tau_1 = \tau_2)$. This equation shows how we can detect gain mismatch. In (7), the magnitude of the denominator becomes constant when the PLL and frequency parameters are fixed. In addition, this equation shows that the loop-filter order only affects the magnitude of the denominator and does not change the relationship between the loop-filter voltage and the injected signal voltage. Hence, the output voltage of the loop filter will follow the pattern of the injected transmit signal depending on the degree of the mismatch. The loop-filter output will show an attenuated transmitted signal with a fixed ratio by (7). For example, when the VCO gain is positive polarity, if the loop-filter output voltage shows the same polarity as the transmit signal, this means that the modulating gain at the VCO port is small, compared with that at the point of the delta–sigma modulator. In other words, we should increase the gain at the VCO port. In contrast, when the polarity between these signals is in antiphase, we should reduce the gain at the VCO path. Fig. 6 and Table I show the summary of the polarity relations between the loop-filter output voltage and the original transmit signal. If the pattern of the voltage variation at the loop filter can be detected and compared with the input transmit signal, we can calibrate this gain and minimize the gain mismatch. Moreover, this technique can be applied in the background during the normal operation, which indicates that nonlinear gain and temperature variation are continuously calibrated and cannot deteriorate the performance. A similar implementation was used in [8] to suppress the quantization noise of the delta–sigma modulator while this work adopted the calibration to minimize the gain mismatch between two-point modulation paths. In addition, while a similar gain calibration was introduced using all-digital PLL, this work is the first transmitter

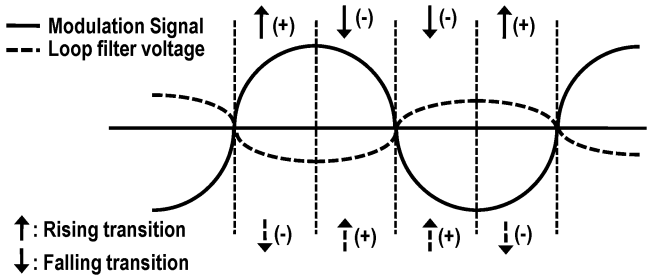


Fig. 6. Waveforms of modulation signal and control voltage in the loop filter when gain mismatch exists.

TABLE I
GAIN OF VCO PATH ACCORDING TO THE MODULATION VOLTAGE AND THE CONTROL VOLTAGE OF THE LOOP FILTER

Loop filter Control voltage	Modulation voltage	Gain of VCO path
+	+	small
–	–	small
+	–	large
–	+	large

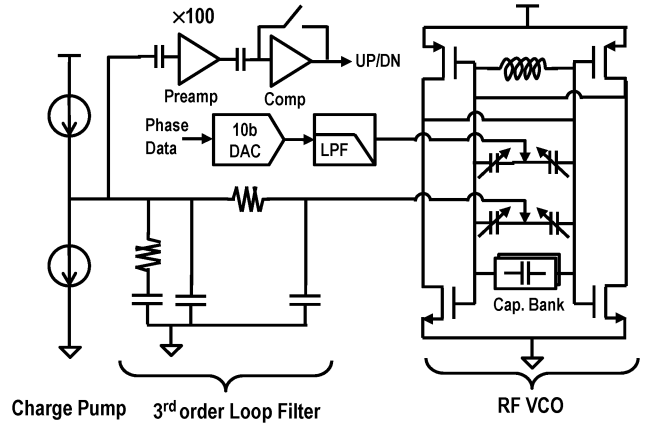


Fig. 7. Schematic of the VCO gain calibration interface.

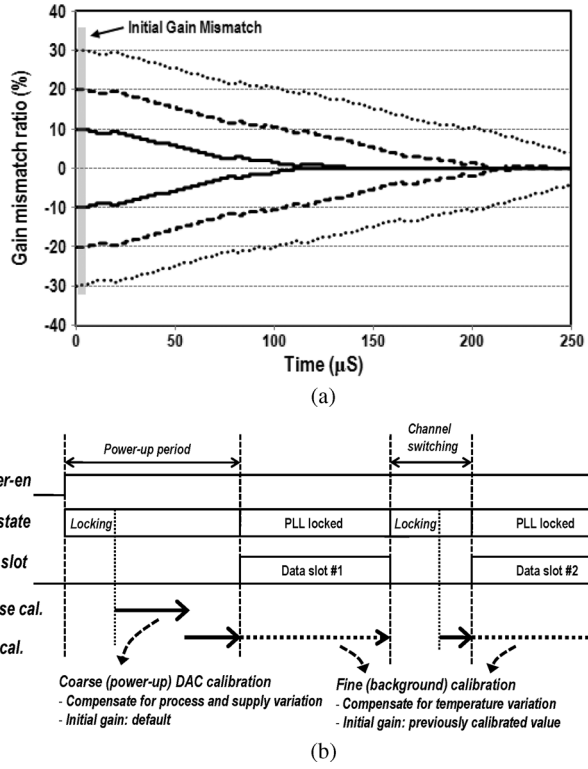


Fig. 8. (a) Transient waveform of gain error convergence. (b) Timing diagram of gain calibration.

architecture using the widely used analog PLL with closed-loop calibration [10], [11].

The comparison between two signals is conducted in the gain calibration block in Fig. 4. The signals coming through two paths (A1 and A2) are compared with each other. The transition directions of the two signals are compared and the gain mismatch is detected. Then, the DAC input is modified by controlling to change the gain on the B2 path. Finally, the gain mismatch between the two signals through the B1 and B2 paths converge to zero. In addition, an extra gain tuning block $\mathrm{MOD_{Amp}}$ is inserted on the B1 path.

Fig. 7 shows the circuit configuration for both the detecting signal voltage at the loop filter and the injecting data at the VCO. According to Fig. 3(b), the simulation result shows that the gain mismatch under 1% satisfies the GSM/EDGE specifications. However, because the amount of the voltage variation at the loop filter is extremely small, detecting the variation caused by the mismatch is difficult. In this configuration, the magnitude of the voltage will be of the order of tens of microvolts at the GSM/EDGE bandwidth. To detect such a small voltage change, a high-accuracy comparator is demanded. The targeted minimum voltage was 5 $\mathrm{mV_{P-P}}$ at the comparator input. Thus, we adopted a very low-noise preamplifier to amplify by 100 times the voltage variation at the loop filter [17]. Before and after the amplification, two ac couplers are utilized for unwanted dc elimination. The ac coupling pole frequency was set to 50 kHz, which was determined in consideration of the GSM signal bandwidth (∼200 kHz). After the amplification and the ac coupler, a two-stage comparator, employing an offset cancellation scheme, compares the incoming signals with time intervals consecutively. The comparison decision was conducted without averaging because the averaging time increases the overall calibration time. The comparison frequency was half of the reference frequency (13 MHz). The comparator compares the present incoming signal with the previous one, so that the signal transition direction can be detected.

Fig. 8(a) shows the gain error convergences in the time domain in a behavioral model simulation, according to the degree of the error. Because the required calibration time linearly depends on the magnitude of the gain error, when the gain error exceeds 30%, the total calibration time takes more than 250 μs. Therefore, using a GMSK test signal that is similar to a single-tone signal, the gain calibration is performed with three steps, as shown in Fig. 8(b). First, a coarse calibration is performed for 300 μs after initial PLL locking for process and supply variation. Through this coarse calibration, the initial gain is estimated. Second, the fine calibration for temperature variation is

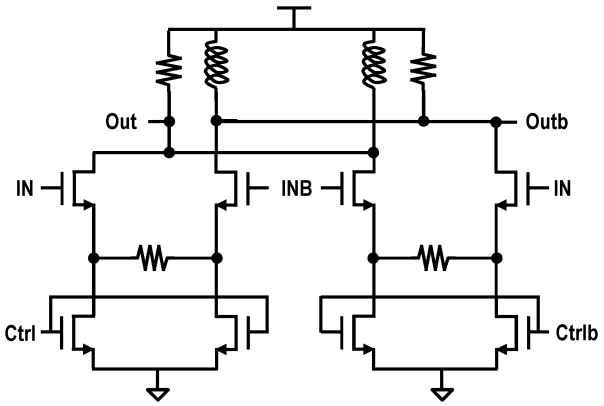


Fig. 9. VGA for AM.

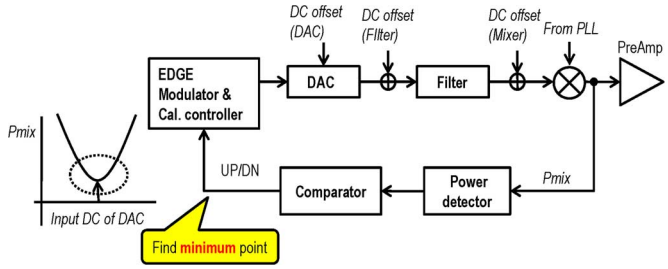


Fig. 10. DC calibration structure.

conducted during 100 μs in the channel switching time. In addition, a background gain calibration is running to minimize subtle gain mismatches. This background calibration loop is performed during normal data communications. The resultant maximum calibrated gain ranges are $+/-30\%$ for coarse tuning and $+/-5\%$ for fine tuning. The gain range can also be increased by increasing the calibration time. The varactor gain of the VCO for modulating the phase signal is set to 3.5 MHz/V, which is selected in considerations of the gain flatness of the varactor and the phase noise of the VCO.

Considering the achievable phase noise and the lock time, the synthesizer loop bandwidth was set to 80 kHz. When the bandwidth is too large, the quantization noise of the delta–sigma modulator will affect the loop-filter output voltage and will limit the effective calibration accuracy. In contrast, if this bandwidth is too small, the calibration time will be too long. However, this relationship between the loop bandwidth and the calibration accuracy and time is not mandatory.

In addition, the interaction between the PLL and the calibration loop should be considered. In order to minimize the effect between the two closed loops, ten is chosen as the bandwidth ratio between the two loops, so that the two loops are guaranteed to operate independently. The resolution of the gain calibration is set to 0.2%, which is limited by the detection accuracy of the output voltage at the loop filter. This resolution guarantees stable EVM performance without the use of any predistortion techniques.

C. DC Calibration

To support the EDGE mode, amplitude modulation is utilized with a VGA. Although the conventional supply modulation method, in which the supply voltage of a driving amplifier or PA is modulated, has a merit of driving a high power level, this technique can make AM–PM and AM–AM problems. Therefore, in this transmitter, an active mixer is used as a VGA for AM. Fig. 9 shows the schematic of the mixer for AM, which is similar to a conventional active mixer. By employing both the linear gain region of input transistors and the degeneration resistances, more linear gain characteristics are achieved. The gain amplification in the VGA is relatively insensitive to AM–PM and AM–AM interactions, because the gain can be controlled in the linear voltage range at the gates of the transistors. The simulation results show that the strong linearity and 0.2° phase deviation over a 400-mV input range are achieved according to the control voltage.

However, when the mixer is adopted as a VGA, the output of the mixer can show an unwanted dc tone as the result of a mismatch between the transistors or by unintended signal coupling from the DAC, the low-pass filter, and the mixer. The dc offset on the envelope path creates a leakage path for the phase-modulated carrier. For example, according to the simulation, when the dc offset mixes the phase-modulated signal, a dc offset of more than 4 mV does not satisfy the EVM specification of EDGE. Therefore, calibration for dc elimination is conducted. The effects of both the magnitude and the phase mismatches are analyzed. According to the behavioral simulation, both the magnitude and phase mismatches are critical for the output carrier leakage problem. The magnitude mismatch leads to the unwanted dc offset at the output of the mixer. The dc offset magnitude is measured by using a monitoring feedback loop, as shown in Fig. 10. The mixer output is monitored by a power detector. If the mixer output contains the carrier leakage, the peak detector will generate an appropriate output and the DAC in the closed loop compensates the dc offset by adding or subtracting digital input. By adjusting the DAC digital input, the minimum envelope signal is detected and the output dc offset of the mixer is minimized by adding the offset value to the DAC.

However, because this method reduces the dc offset with an additional dc signal, the dc offset from the phase mismatch cannot be clearly compensated for. Thus, although the dc offset calibration for the magnitude mismatch is conducted, the output dc offset of the mixer remains more than 30 mV under the 3° phase mismatch between the LO signals. Therefore, the phase mismatch should be calibrated in another way. Fig. 11(a) shows the tuning blocks of the LO input path. By adjusting the *RC* time constant at the input biasing resistor network using switches, we can control the LO phase mismatch. If the LO biasing resistance on the one side is 20 KΩ, then the resistance on the opposite side can be changed according to the phase mismatch, as shown in Fig. 11(b). It shows that the dc offset due to the LO phase mismatch can be compensated for by selecting the proper resistor at the input biasing circuit.

Therefore, as shown in Fig. 12, the whole dc calibration is conducted in three steps. Because dc calibration is not strongly dependent on the PLL locking, this calibration is conducted during the guard time for switching between the two channels. The dc calibration procedure is performed as follows. First, after a short time margin, adding/subtracting the digital offset to the

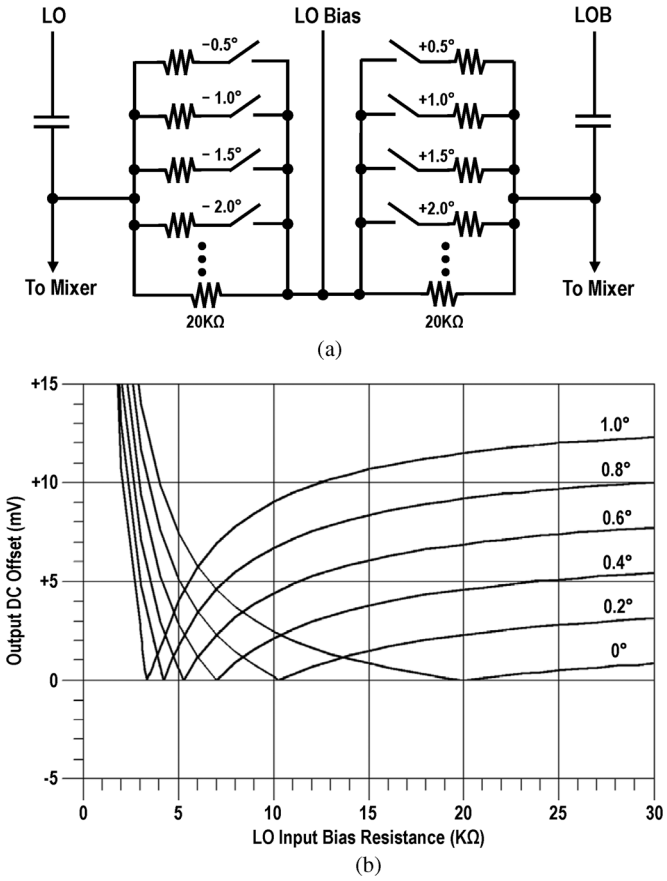


Fig. 11. Phase-mismatch calibration: (a) input biasing circuit using tunable resistors; (b) dc offset variation according to LO input bias resistance under various LO phase mismatches.

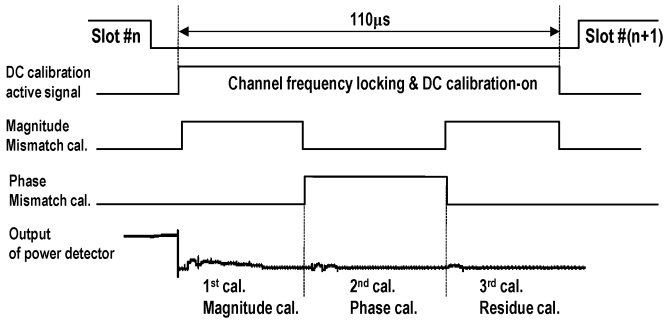


Fig. 12. DC calibration timing diagram.

DAC input finds the minimum output of the power detector. Second, to minimize the dc offset from the LO phase mismatch, the optimum resistor in the LO input biasing block is found by monitoring the output power of the power detector. Finally, the digital offset calibration using the DAC performed in the first calibration is conducted again, because the resistance imbalance resulting from the second calibration block can create an LO amplitude mismatch. The accuracy of this dc calibration is 1 mV, which is limited by the 10-bit DAC resolution. That corresponds to −52 dBc of carrier leakage. Through this calibration, we achieve robust AM against the magnitude and phase mismatch.

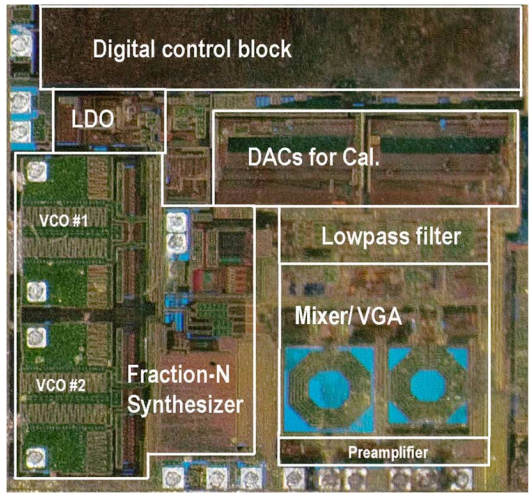


Fig. 13. Chip microphotograph.

TABLE II
TRANSMITTER PERFORMANCE SUMMARY

	GSM		EDGE	
Frequency band	Low (850/900)	High (1800/1900)	Low (850/900)	High (1800/1900)
Maximum output power	2 dBm	2 dBm	2 dBm	1 dBm
Modulation spectrum 400kHz 600kHz	 -66 dBc -79 dBc	 -65 dBc -78 dBc	 -67 dBc -73 dBc	 -66 dBc -71 dBc
RMS phase error	1.9°	2°	2.5°	2.8°
Noise 10MHz offset	-155 dBc	-146 dBc	-152 dBc	-144 dBc
Noise 20MHz offset	-164 dBc	-154 dBc	-164 dBc	-153 dBc
RMS EVM	< 2 %	< 2 %	< 2 %	< 3.5 %
Current	76 mA	74 mA	89 mA	91 mA

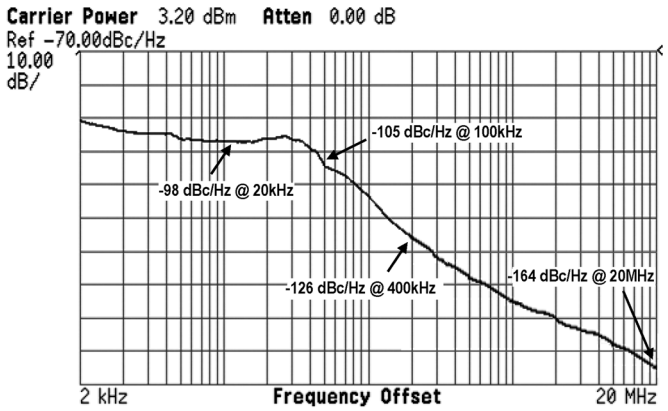
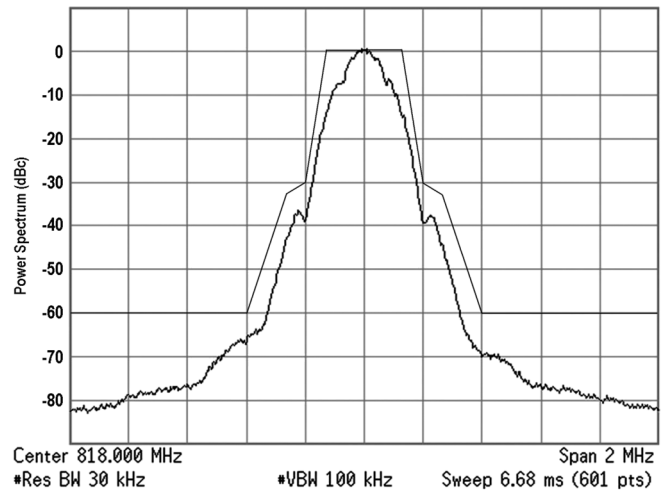


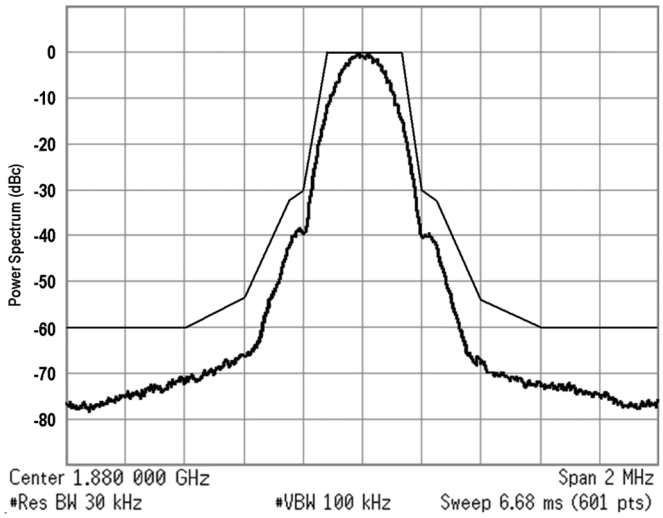
Fig. 14. Measured phase noise levels at GSM900 mode.

IV. MEASUREMENT RESULTS

The proposed two-point modulation technique has been verified in the GSM/EDGE transmitter using 0.25-μm one-poly five-metal CMOS technology. Fig. 13 shows a microphotograph of the transmitter, which occupies an area of 3.5 mm^2, including the bonding pads. A regulator for the digital control block and two DACs is put into place to suppress the unwanted coupling

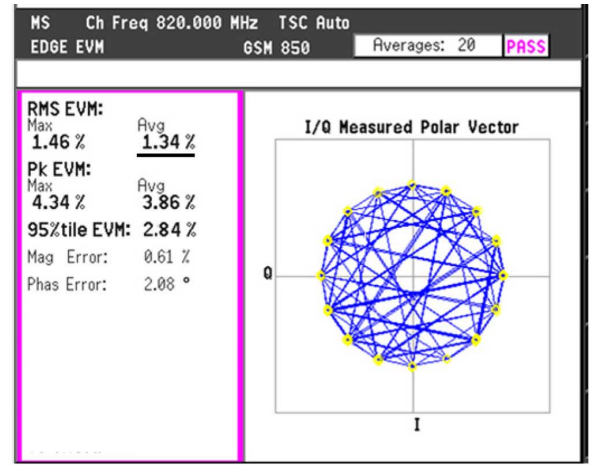


(a)

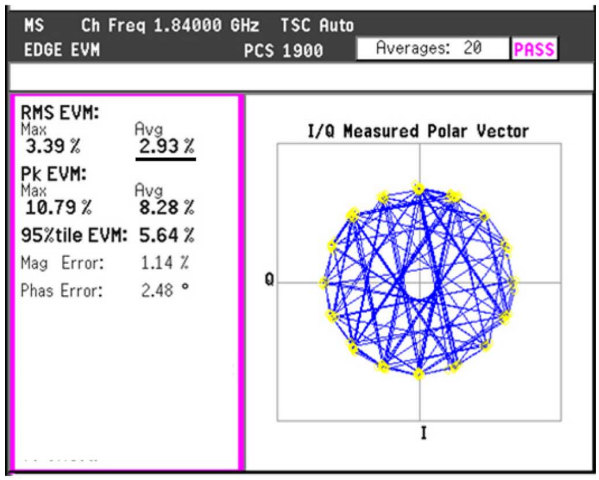


(b)

Fig. 15. Modulated spectrum at output of transmitter: (a) GMSK-modulated output at low band; (b) EDGE output at high band.



(a)



(b)

Fig. 16. EVM performance of EDGE transmitter: (a) low band; (b) high ban.

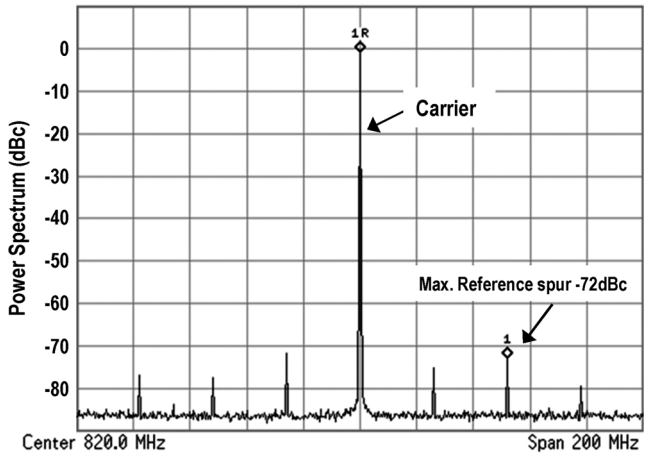


Fig. 17. Spurious emission in TX output.

noise to the RF blocks. In addition, to improve the isolation between blocks, deep trenches and guard rings are added to the layout. We have also extensively used the two top metal layers of the process with the metal–insulator–metal (MIM) capacitor in order to provide a better decoupling characteristic. The two VCOs utilized bondwires for inductors with pad-to-pad connections. The transmitter performance is summarized in Table II. For the measurement of the transmitter, measured phase-noise levels at GSM900 mode are shown in Fig. 14. The spectrum measured in the output of the transmitter shows the 80-kHz bandwidth and the phase noise at each frequency specification. With the optimized sizing in the charge pump for low noise, low in-band phase noise of -98 dBc/Hz is achieved. The third-order loop filter and low-phase-noise VCO lowered the noise to -164 dBc/Hz at a 20-MHz frequency offset, which is the most stringent specification of the GSM low band. The measured transmitted signal spectrums of the GSM low band and the EDGE high band, when delivering 2 dBm into a 50-Ω load, are shown in Fig. 15. The spectrum masks conform to the GSM and EDGE masks within a safe margin at the maximum output power. Fig. 16 shows the EVM measurement results of EDGE with both modes at maximum output power. There was no large sideband tone to exceed the TX EVM specification, so that the TX EVM was found to be less than 2% and 3% rms at the high and low bands, respectively. Spurious emissions in the TX output are 72 dB below the desired signal, as shown in Fig. 17.

TABLE III
COMPARISON WITH PREVIOUS GSM/EDGE CIRCUITS

	Process	Block	supply voltage	Current / Power consumption	20MHz Offset Noise	RMS EVM (EDGE LB)	Size	Note
[1] 2002 JSSC	0.35-μm BiCMOS	TX+RX	2.7 V	TX: 130 mA	-164dBc/Hz	-	-	OPLL
[2][1] 2008 ISSCC	0.13-μm CMOS	TX+RX	1.5/2.7 V	TX: 285 mW	-165dBc/Hz	2.2%	-	ΣΔ-modulation (one-point)
[4] 1999 JSSC	Bipolar	TX+RX	2.7 V	-	-165dBc/Hz	-	11.6 mm^2	OPLL
[5] 2004 JSSC	0.5-μm BiCMOS	TX	-	75 mA	-164dBc/Hz	3%	7.8 mm^2	OPLL
[12] 2005 JSSC	0.09-μm CMOS	TX	1.2 V	EDGE: 42 mA	-165dBc/Hz	1.2%	1.5 mm^2	ADPLL
[16] 2009 SOVC	0.11-μm CMOS	TX	-	GSM: 54 mA	-165dBc/Hz	-	1.8 mm^2	ΣΔ-modulation (one-point)
[18][2] 2004 JSSC	0.35-μm BiCMOS	TX+RX	2.7 V	-	-165dBc/Hz	2.9%	20 mm^2	OPLL
[19][1] PM6272	0.13-μm CMOS	TX	1.4-2.95 V	TX: 289 mW	< -161.5dBc/Hz	2.5%	-	ΣΔ-modulation
[20] 2009 JSSC	0.13-μm CMOS	TX+RX	2.8 V	TX: 118 mA	-164dBc/Hz	1.9%	-	Direct Up-Modulation
This work	0.25-μm CMOS	TX	2.7 V	EDGE: 92 mA GSM: 74 mA	-164dBc/Hz	1.34%	3.5 mm^2	ΣΔ-modulation (two-point)

[1] Current consumption is not shown.
[2] PA is included.

A comparison with previous circuits is summarized in Table III. The previous transmitters used by OPLL and direct up-conversion draw larger current than the two-point modulation technique. Although this GSM/EDGE prototype is fabricated using a relatively low-cost process, 0.25-μm, it showed very low EVM performance, which is comparable to the lowest EVM result. As a result, combining the widely used analog PLL, this proposed two-point modulation technique achieves solid performance.

V. CONCLUSION

We have demonstrated a new self-calibration two-point modulation technique for a CMOS transmitter. This technique minimizes the gain and timing mismatches between two modulation points, which can cause wideband phase modulation. In addition, dc calibration for amplitude modulation in polar loop provides a stable output spectrum with low carrier leakage. The GSM/EDGE transmitter adopting the proposed technique leads to a simple transmitter architecture, stable EVM performance with low cost, and the possibility of multiband functionality. This offers an advantage in transmitters by using two-point modulation: a low-cost, low-power transmitter solution.

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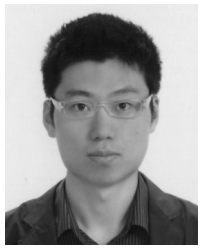

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