A Low-Phase-Noise 77-GHz FMCW Radar Transmitter With a 12.8-GHz PLL and a ×6 Frequency Multiplier

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***Abstract*—In this letter, a 77-GHz transmitter (TX) with a 12.8-GHz phase-locked-loop (PLL) and a ×6 frequency multiplier is presented for a FMCW radar sensor in a 65-nm CMOS process. To realize the low-phase-noise TX, a voltage controlled oscillator (VCO) with an excellent phase noise performance at a lower fundamental frequency (12.8 GHz) is designed and scaled up (×6) for the desired target frequency (77 GHz). The measured FMCW modulation range with an external triangular chirp signal (1-ms sweep time) is 601 MHz. The output power and the total DC power consumption of the TX are 8.9 dBm and 116.7 mW, respectively. Here, a good phase noise level of −91.16 dBc/Hz at a 1-MHz offset frequency from a 76.81-GHz carrier is achieved.**

***Index Terms*—Frequency multiplier, frequency-modulated-continuous-wave (FMCW) radar transmitter, phase-locked loop (PLL), 77-GHz.**

I. Introduction

In millimeter (mm)-wave frequencies, SiGe technologies have been widely used from the past due to high cut-off frequency and breakdown voltage [1]–[3]. With the recent performance development of CMOS devices, CMOS can be applied to mm-wave radar systems [4]–[6]. Although CMOS radar systems have some advantages, such as low cost and high integration, the phase-noise performance should be improved further in order to compete with SiGe radar systems. Thus, achieving a low-phase-noise signal generator in CMOS has been a significant issue.

Several approaches to designing a low-phase-noise 77-GHz FMCW signal generator are employed in this paper. At mm-wave frequencies, a VCO suffers from high phase noise due to poor transistor gain as well as the low quality factor of varactors. Therefore, despite consuming more DC power, combining a lower frequency VCO and a frequency multiplier can be a more appropriate solution than direct mm-wave oscillation for the mm-wave low-phase-noise performance [7]. Considering the system implementation issues such as the frequency lock ranges, DC power consumption, and VCO performance, the multiplication factor is set to 6 in this research. In addition, the proposed 77-GHz signal generator (a VCO, a buffer, a tripler, and a doubler) is designed with an injection-locked (IL) oscillator (ILO) chain, which is a powerful tool to realize low-phase-noise oscillators with good harmonic suppression at mm-wave frequencies [8]. Because the phase noise of the ILO chain is determined by injected signal purity, the lower frequency VCO is designed with a linearized transconductance (LiT) technique which shows low-phase-noise performance [9].

Using these approaches, a 77-GHz FMCW radar TX based on a low-phase-noise 12.8-GHz PLL and a ×6 multiplier is shown in this paper.

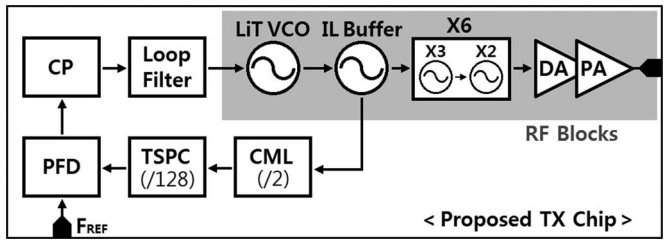

Fig. 1. Block diagram of the proposed 77-GHz TX chip.

II. Architecture and Circuit Description

The block diagram of the proposed 77-GHz radar TX is shown in Fig. 1. It consists of a 77-GHz signal generator, a driver amplifier, a power amplifier and PLL blocks. Because the signal generator is implemented with the ILO chain without requiring gain buffers after each ILO, the DC power consumption and chip area can be decreased. Moreover, harmonic suppression, which is one of the main concerns of the multiplier-based system, can be improved by the ILO chain because each oscillator acts as a narrow band-pass filter.

A conventional integer-N PLL is used to precisely define the output frequency of the VCO. It is composed of a current-mode logic (CML) divider, seven stages of true-single-phase-clock (TSPC) divider, a phase frequency detector (PFD), a charge pump (CP), and a loop filter. The PFD compares phase and frequency of the divided VCO output signal to those of a reference signal (F_{REF}). The loop bandwidth can be adjusted from 100 kHz to 1 MHz by controlling the CP bias current.

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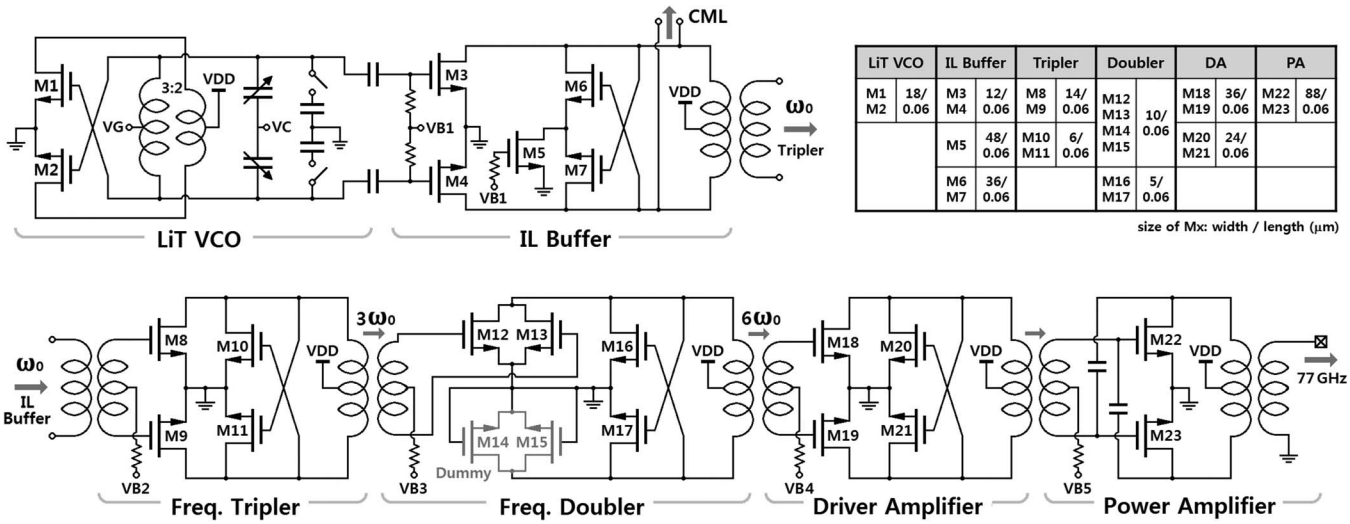


LiT VCO		IL Buffer		Tripler		Doubler		DA		PA	
M1 M2	18/ 0.06	M3 M4	12/ 0.06	M8 M9	14/ 0.06	M12 M13 M14 M15	10/ 0.06	M18 M19	36/ 0.06	M22 M23	88/ 0.06
		M5	48/ 0.06	M10 M11	6/ 0.06			M20 M21	24/ 0.06		
		M6 M7	36/ 0.06			M16 M17	5/ 0.06				

size of Mx: width / length (μm)

Fig. 2. Circuit schematic of RF blocks.

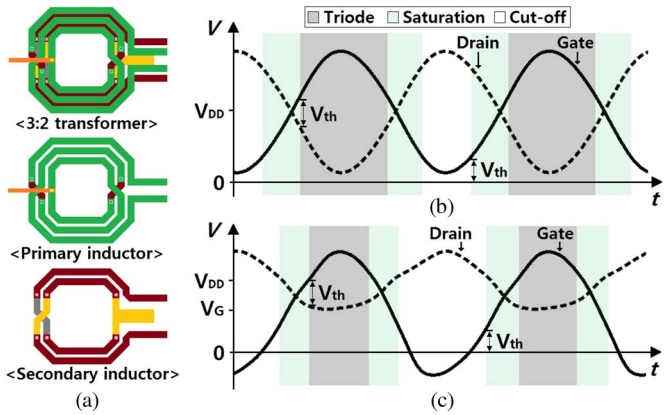


Fig. 3. (a) Designed 3:2 transformer for a LiT VCO, (b) simulated waveforms of a conventional LC VCO, (c) those of a 3 : 2 transformer based LiT VCO.

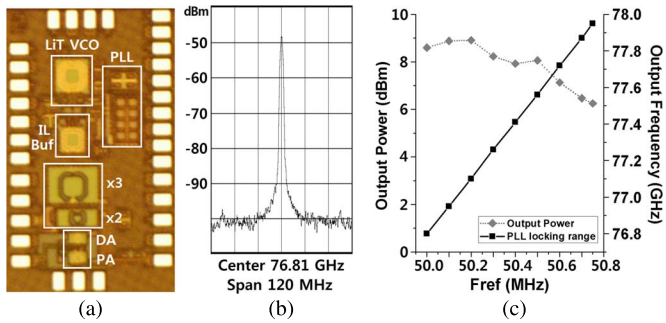


Fig. 4. (a) Chip micro-photo, (b) measured output spectrum of the 77-GHz TX, (c) measured output frequency and power.

A detailed schematic of RF blocks is presented in Fig. 2. It is generally known that the VCO phase noise is fundamentally limited by the oscillation amplitude and inherent device noise. The LiT technique has been recently reported to solve these problems. A different feedback concept, which has a lower voltage swing on the drain node than on the gate node, is required for the LiT. The previous LiT VCO is realized using a capacitive divider network for the LiT feedback and a bulky choke inductor at the drain due to an LC tank at the gate [9]. However, those complex and bulky components are readily replaced with a 3 : 2 transformer in the proposed VCO [Fig. 3(a)] [10]. To realize the lower voltage swing on the drain node than on the gate node, the primary three-turn inductor and secondary two-turn inductor are connected to the gate and the drain of M1/M2, respectively. The simulated gate and drain waveforms of a conventional LC VCO and the 3 : 2 transformer-based LiT VCO are shown in Fig. 3(b) and (c). The triode region, which is one of the main cause of VCO nonlinearity, can be reduced by lowering the drain voltage swing.

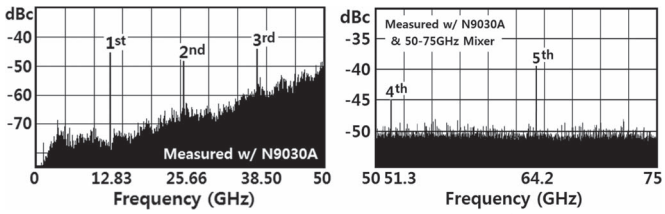
The IL buffer, which oscillates at ω_0 (12.8 GHz), consists of a small-sized M3/M4 that injects the VCO signal into the buffer, a current source (M5), a large-sized cross-coupled M6/M7 for generating a high output power, and a transformer. The sub-harmonic components coupled from the CML divider may modulate the VCO. However, the IL buffer which operates as a narrow band-pass filter can suppress them.

The ×6 frequency multiplier is composed of the tripler and doubler that are designed with the IL oscillator. The third harmonic signal is injected through M8/M9 to the tripler core, which oscillates at 3 ω_0 (38.5 GHz) [11]. Thus, the $3\omega_0$ signal is coupled through the tripler transformer to the doubler input. The frequency doubling is implemented using the push-push differential pair (M12/M13) that generates the second harmonic signal at the common drain node of M12/M13. Then, this second harmonic signal is injected into the doubler core, which oscillates at $6\omega_0$ (77 GHz). The dummy differential pair (M14/M15) is used to improve the doubler output balance.

The 77-GHz output signal of the ×6 multiplier is coupled to the DA using a transformer. The DA includes a cross-coupled pair (M20/M21) to boost the signal swing with a low DC power consumption. The cross-coupled neutralization capacitance between the gate and drain of M22/M23 is applied to guarantee the stability as well as the PA gain [12].

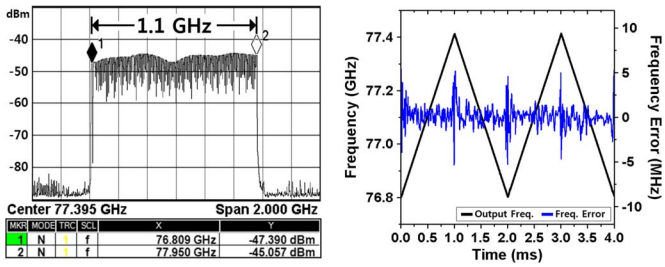
III. Measurement Results

The proposed circuit is fabricated via a standard 65-nm CMOS process. Fig. 4(a) shows a micro-photograph of the proposed 77-GHz radar TX chip. The total chip area is 1.38 × 0.79 mm^2. Spectrum of the TX output when the output signal (76.81 GHz) is locked by a 50-MHz reference signal is shown in Fig. 4(b). The maximum measured output power is 8.9 dBm



(a) (b)

Fig. 5. Output spectrums of the harmonics in (a) 0–50 GHz, (b) 50–75 GHz.



(a) (b)

Fig. 6. (a) Spread spectrum, (b) FMCW profile and frequency error.

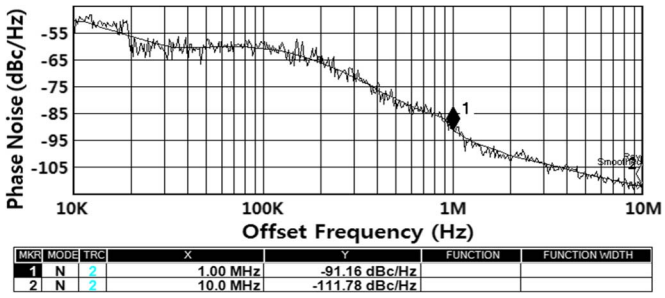


Fig. 7. Measured phase-noise at 76.81-GHz carrier frequency.

(Agilent N1914A power meter) when the TX total DC power consumption is 116.7 mW, as presented in Fig. 4(c). The 1st, 2nd, and 3rd harmonic output spectrum is presented in Fig. 5(a) and the 4th and 5th harmonic components are shown in Fig. 5(b). Due to the ILOs, the undesired harmonic components are lowered below −39 dBc. Fig. 6(a) shows the measured 76.81–77.96-GHz spread spectrum under a 50–50.75-MHz PLL reference clock. Because fast sweep time of an external triangular chirp signal is required for the automotive FMCW radar application, the measured FMCW chirp bandwidth is lowered to 601 MHz with a 1-ms sweep time, as shown in Fig. 6(b). The measured root-mean-square (rms) frequency error is approximately 490 KHz. In Fig. 7, the measured phase noise shows a great value of −91.16 dBc/Hz at a 1-MHz offset when the loop bandwidth is 100-KHz (Agilent N9030A). The phase noise at 12.8-GHz test point (free-running LiT VCO) is −114 dBc/Hz at the 1-MHz offset. With this 12.8-GHz signal source, the ideal estimated phase noise at 76.8-GHz carrier is −98.4 dBc/Hz $(-114 + 20\log 6)$. However, the phase noise is degraded to −91.16 due to the injected noise from the multiplier chain. Table I highlights the comparison of this work with recently published works.

IV. Conclusion

The low-phase-noise 77-GHz radar TX in 65-nm CMOS is presented in this paper. The proposed TX chip employs a suitable multiplier-based structure and a 12.8-GHz LiT VCO to achieve low phase noise. Moreover, the ILO chain is applied to the frequency generator to decrease the chip area and DC power consumption and to suppress undesired harmonics from lower frequency blocks. Therefore, the phase-noise performance value as low as −91.16 dBc/Hz at a 1-MHz offset frequency with a 76.81-GHz carrier and DC power dissipation as low as 116.7 mW while generating the 8.9-dBm output power.

TABLE I
Comparison of Radar Transmitters or Transceivers

	[2]	[3]	[4]	[5]	[6]	This
Tech.	SiGe Bipolar	SiGe Bipolar	65nm CMOS	90nm CMOS	65nm CMOS	65nm CMOS
Func. / PLL	TRX / Frac. N	TRX / –	TRX / Frac. N	TRX / Int. N	TX / Frac. N	TX / Int. N
Freq. (GHz)	68–93.6	75–79	75.6 –76.3	78.1 –78.8	76–81	76.81 –77.95
RMS Freq. Error (KHz)	N/A	N/A	< 300	N/A	970	490
×N	×1	×18	×1	×1	×2	×6
P_{out} (dBm)	7	6.2	5.1	-2.8	3	8.9
Phase Noise (dBc/Hz)	-88@10K -90@1M	-105.3* @1M	-85.33 @1M	-85 @1M	-83.43 @1M	-91.16 @1M
TX+ PLL Pdiss (mW)	423	1125	243 (TRX)	406	320	116.7
Area (mm^2)	1.9×1.6	3×1.8	1×1.1	3.5×2	1.5×1.9	1.4×0.8

* 4.25-GHz external signal source (Agilent E8257D) is used.

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