A Blocker-Tolerant Double Noise-Cancelling Wideband Receiver Front-End Using Linearized Transconductor

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***Abstract*—In this paper, a wideband receiver front-end using a linearization technique of transconductor is presented. A low-noise transconductance amplifier is designed to perform both linearization and noise cancellation simultaneously, achieving high input-referred third-order intercept point (IIP3) values and low noise figure. In addition, a wideband input matching and a second noise cancellation technique using a feedback path and an auxiliary path are applied. The designed wideband receiver, fabricated in 65 nm technology, operates in the 0.06-3 GHz frequency band and has a gain of 52.7 dB, a minimum noise figure of 1.4 dB, and a maximum IIP3 of 5.15 dBm.**

***Index Terms*—Wideband receiver, blocker, linearity, transconductor linearization, noise cancellation.**

I. Introduction

The frequency spectrum is now reaching saturation due to the various communication standards. Generally, each standard requires a dedicated narrowband receiver, and wireless communication devices, especially mobile phones, contain multiple receivers to support standards such as cellular communication, Wi-Fi, Bluetooth, GPS and so on. This increases the area and cost of the mobile phone. Thus, attempts have been made to support multiple standards with a single wideband system [1]-[3].

Because wideband receivers cannot use RF band-pass filters such as surface acoustic wave (SAW) filters, out-of-band interferer signals, or blockers, are the biggest problem. There are two problems caused by the blocker. First, the receiver itself can be saturated because of the large blocker. Secondly, there is a possibility that intermodulation components by two or more large blocker signals may distort the in-band signals. In this paper, the current-mode receiver structure is used to prevent the saturation of the receiver by the blocker and suppress the generation of the intermodulation component using the linearization technique of the low-noise transconductance amplifier. In addition, we propose a double noise canceling method to improve the noise figure performance of the receiver as well as enable wideband operation.

II. Receiver Design

A common architecture for wideband receivers is the current-mode receiver [4]. This structure uses a low-noise transconductance amplifier (LNTA) instead of a conventional low-noise amplifier (LNA) as an amplification element in RF. Here, LNTA has the advantage of preventing the saturation of the receiver by the blocker, by converting the input voltage into the current proportional to the transconductance value. The output current of LNTA is downconverted to baseband by a passive mixer. Then, the baseband current is converted

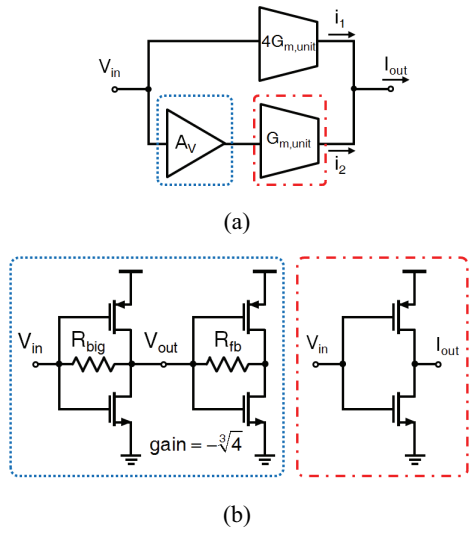

Fig. 1. (a) Block diagram of linearized transconductor. (b) Schematics of the voltage amplifier and unit transconductor.

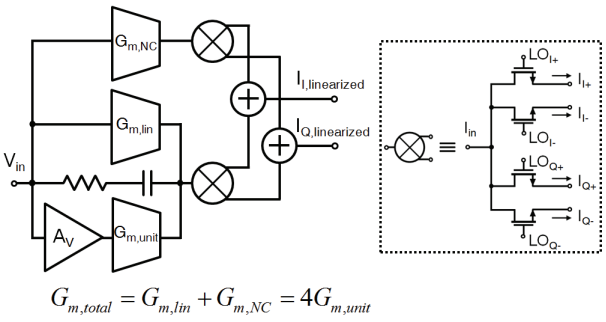

Fig. 2. Block diagram of linearized noise-cancelling technique and schematic of passive mixer.

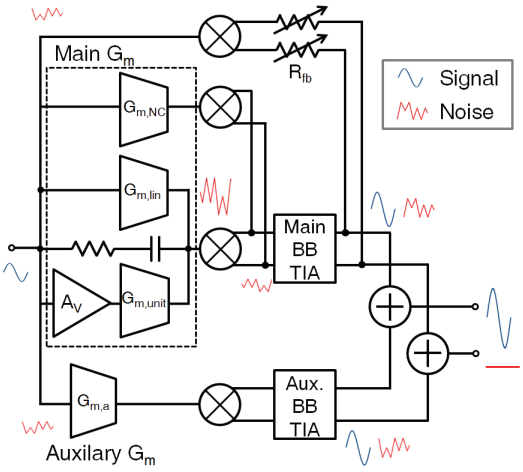

Fig. 3. Schematic of the double noise-cancelling receiver front-end.

to voltage output. It should be noted that the input impedance of the mixer and baseband transimpedance amplifier (TIA) connected to the LNTA must be kept low to minimize unwanted voltage swing. In addition, it is necessary to operate the LNTA very linearly to prevent intermodulation due to the blocker. Therefore, a technique of linearization to prevent the generation of the third-order intermodulation distortion (IMD3) component in the LNTA will be explained first.

A. Linearized Noise-Cancelling LNTA

Linearization technique has been proposed to suppress IMD3 components generated in LNTA [5]-[7]. In the proposed method, the input voltage and output current of the transconductance amplifier are approximated as $I_{out} \approx G_{m1}V_{in} + G_{m3}V_{in}^3$. Here, G_{m1} represents the fundamental transconductance of the transcondcutor, and G_{m3} represents the term for generating the IMD3 component. The linearization circuit consists of two paths, and by adding the output current in each path, the linearization is achieved by cancelling the third-order term. Fig. 1 shows a block diagram of a linearized LNTA. The output current for the input voltage in Fig. 1 can be expressed as follows :

$$\begin{aligned} I_{out} &= i_1 + i_2 \\ &= 4G_m V_{in} + 4G_{m3}^3 V_{in}^3 + (-\sqrt[3]{4}G_m V_{in} - 4G_{m3}^3 V_{in}^3) \\ &= (4 - \sqrt[3]{4})G_m V_{in}. \end{aligned} \quad (1)$$

It can be seen from the above equation that the IMD3 component is removed and a linear V-I conversion takes place, but the noise figure performance drops due to the additional circuitry used to achieve linearization. To improve this, a noise-cancelling method in the RF band is applied [8]. This method feeds back the noise at the output node and amplifies it with another transconductor to cancel it. The proposed noise canceling LNTA is shown in

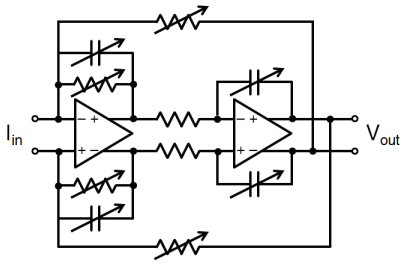

Fig. 4. Schematic of the baseband TIA.

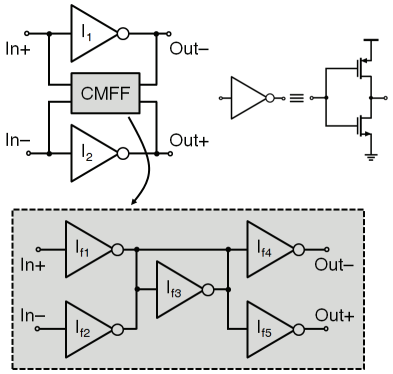

Fig. 5. Block diagram of the differential amplifier and common-mode control circuits.

Fig. 2. The LNTA of the main path is divided into two, and the sum of the total G_m is designed to be $4G_{m,unit}$. As a result, the G_m ratio of the transconductors in the main path and the auxiliary path is kept at 4:1, and the cancellation of the noise occurs in the baseband after downconversion. This circuit structure can achieve both linearization and noise cancellation of the transconductor, and it can alleviate the performance degradation caused by the blocker. In addition, the configuration in which two mixers are connected in parallel has the same effect as reducing the resistance of the mixer in half, and has the advantage of reducing the voltage swing before the TIA. Adjustment of the $G_{m,lin}$ and $G_{m,NC}$ values can cancel the noise from the lower path (voltage amplifier, $G_{m,unit}$, and $G_{m,lin}$), so that $G_{m,NC}$ is the dominant contributor to noise.

B. Wideband Double N.C. Receiver Front-End

A wideband receiver was designed using the linearized noise cancelling LNTA. Fig. 3 is a block diagram of the wideband receiver with a double noise cancelling scheme. A linearized LNTA is used as the main G_m and a feedback path in the baseband is added using the resistor R_{fb}. This path can be used to feedback the noise in the baseband to the RF input node while achieving wideband input matching [2]. The input impedance of the circuit which the feedback is added becomes :

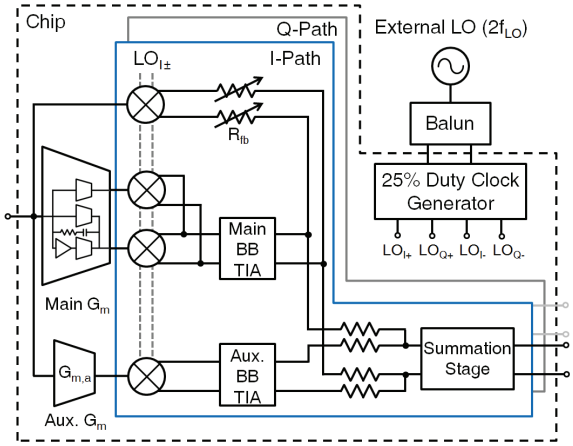

Fig. 6. Schematic of the entire receiver front-end.

$$Z_{in}(\omega_{LO}+\Delta\omega) \approx \frac{\pi}{2\sqrt{2}} \frac{R_{fb}}{1+G_m \frac{\sqrt{2}}{\pi} Z_{BB}(\Delta\omega)}, \quad (2)$$

where $\Delta\omega$ is the offset from the center frequency and Z_{BB} is the transimpedance value. Z_{BB} is adjustable by varying the feedback resistance of the TIA, and controlling R_{fb} can achieve 50 ohm input matching over wideband.

Next, a second noise cancellation operation is enabled by adding an auxiliary path to the receiver circuit. The RF noise that has not been completely removed in the LNTA stage (noise due to $G_{m,NC}$) and noise from the baseband TIA are upconverted back through R_{fb} and removed by combining in the baseband via the auxiliary path.

Fig. 4 shows the circuit diagram of the baseband TIA. It consists of two stages, a circuit based on the Tow-Thomas biquad filter. The attenuation of the blocker signal can be further increased through the second-order filtering operation. It is designed to adjust the gain and bandwidth of the TIA by changing the feedback resistor and capacitor values. A block diagram of the amplifiers in the TIA is shown in Fig. 5. It is made up of pseudo-differential amplifiers, and all the components are designed using simple inverters. This can maintain high linearity in the baseband, and suppresses the effect of flicker noise by using a long channel transistor. In addition, a common mode control circuit consisting of inverters is designed [9].

The structure of the entire receiver is shown in Fig. 6. The chip includes a main LNTA, auxiliary LNTA and mixers, and baseband TIAs with a clock generator. The clock generator is designed using a current mode logic (CML) type divider and requires an external signal of $2f_{LO}$.

III. Measurement Results

The designed chip was fabricated using 65 nm standard CMOS process. The total chip size is 890 um × 820 um and the active area is 650 um × 640 um. Fig. 7 is a

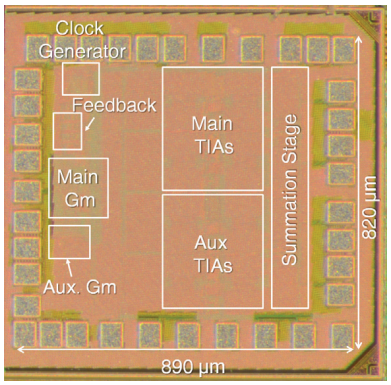

Fig. 7. Chip die micrograph.

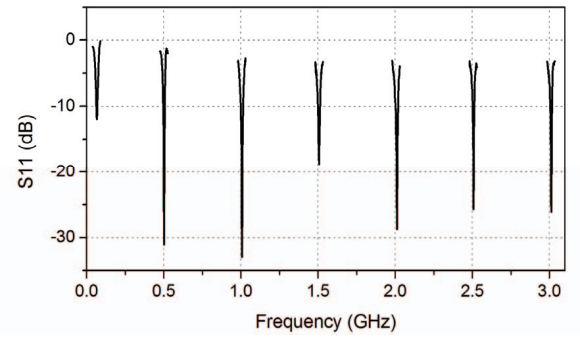

Fig. 8. Measurement result of input matching characteristic.

micrograph of the chip. The supply voltage is 1.2 V and the current consumption is 37-63 mA. In LNTA and baseband TIA, 34 mA is constantly consumed and current consumption increases as the LO frequency increases.

The operation frequency range of the receiver based on the S_{11} value (S_{11} < -10 dB) was measured from 60 MHz to 3 GHz, and the results are shown in Fig. 8. This shows that the input is well-matched to 50 ohm due to the feedback architecture. Fig. 9 shows the gain and noise figure for the LO frequency changes. The gain is 52.7 dB at low frequency, but gradually degrade as the frequency increases. The noise figure shows a low value of 1.4 dB at the low frequency side, but the performance also decreased with increasing frequency.

Fig. 10 shows the linearity measurement results of the receiver at 500 MHz. The input-referred second-order intercept point (IIP2) and IIP3 values of the receiver were measured using a two-tone signal. For IIP2 measurements, the frequencies used are $f_1=f_{lo}+\Delta f$ and $f_2=f_{lo}+\Delta f+800\ kHz$, respectively. For IIP3 measurements, $f_1=f_{lo}+\Delta f$ and $f_2=f_{lo}+2\Delta f+800\ kHz$ were used. A high IIP3 value of 5.15 dBm was obtained using the linearized LNTA. The IIP2 value was larger than 40 dBm in the out-band.

The measurement results are summarized in Table I and compared with the results of previous studies. This

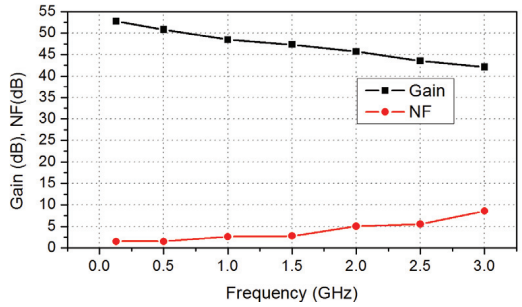

Fig. 9. Measured gain and noise figure.

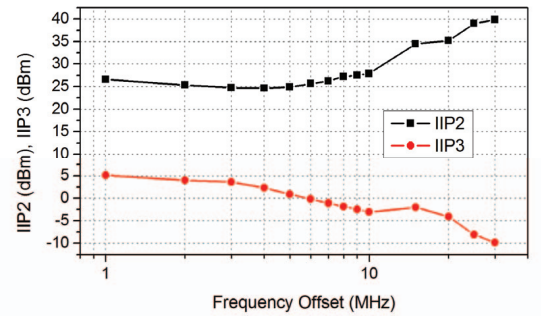

Fig. 10. IIP2 and IIP3 measurement results.

design has the widest fractional bandwidth in the operating frequency section. The linearized LNTA and double noise cancellation technique can achieve the lowest minimum noise figure and good IIP3 value.

IV. Conclusion

By improving the linearization technique of the transconductor, an LNTA that can perform linearization and RF noise cancelling simultaneously is designed. Then, a second noise cancellation is performed by adding the feedback and the auxiliary path. The entire receiver circuit consisted of inverter circuit, resistor, and capacitor, and showed wideband operation characteristics. The proposed receiver achieves a high IIP3 value by the linearization technique and a low noise figure by the noise canceling technique, which is suitable for a wideband receiver which must withstand an external blocker.

Acknowledgment

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TABLE I. Performance Summary and Comparison

	[1]	[2]	[3]	**This work**
Type	Noise Cancelling	Noise Cancelling	N-path Filter	Double N.C.
Frequency (GHz)	0.08-2.7	0.7-3.8	0.1-2	0.06-3
Gain (dB)	72	42	16	52.7
NF (dB)	1.9	1.6-3.2	4.1-10.2	1.4-8.5
IIP3 (dBm)	13.5	1	44	5.15
IIP2 (dBm)	54	> 75	90	40
Supply Voltage (V)	1.3	1.2	1.2/1.0	1.2
Current (mA)	35.1-78	22.8-34.9	36.6-90	37-63
Active Area (mm^2)	1.2	0.15	0.49	0.42
Process (nm)	40	65	28	65

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