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PAPER

Design Optimizaion of Gm-C Filters via Geometric Programming

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SUMMARY This paper presents a design optimization method for a Gm-C active filter via geometric programming (GP). We first describe a GP-compatible model of a cascaded Gm-C filter that forms a biquadratic output transfer function. The bias, gain, bandwidth, and signal-to-noise ratio (SNR) of the Gm-C filter are described in a GP-compatible way. To further enhance the accuracy of the model, two modeling techniques are introduced. The first, a two-step selection method, chooses whether a saturation or subthreshold model should be used for each transistor in the filter to enhance the modeling accuracy. The second, a bisection method, is applied to include non-posynomial inequalities in the filter modeling. The presented filter model is optimized via a GP solver along with proposed modeling techniques. The numerical experiments over wide ranges of design specifications show good agreement between model and simulation results, with the average error for gain, bandwidth, and SNR being less than 9.9%, 4.4%, and 14.6%, respectively.

key words: *ultra-low power, optimization, geometric programming, subthreshold mode operation, active filter*

1. Introduction

Active Filters are principal building blocks in modern radio frequency (RF) and baseband systems. Channel select filters [1] and image-rejection filters [2] are routinely designed using active filters. The design of an active filter has to consider intricate tradeoffs among power, gain, bandwidth, noise, and linearity, among others. To address such design complexity, many design optimization methods have been proposed. A genetic algorithm [3]–[5] has been used to optimize active filters, and a general matrix-based approach [6] has been applied to design continuous-time filters. Specific design parameters, such as dynamic range and stability, can be optimized by various algorithms [7]–[9]. While those papers address various challenges in an active filter design mainly at architecture-level, the result of optimization does not seamlessly lead to a fully optimized transistor-level filter design.

In this paper, we present an active filter optimization method based on geometric programming (GP), a special kind of convex optimization that has shown viability in optimizing various analog circuits at all levels of design hierarchies [10]–[13]. Our specific focus is the design optimization of a Gm-C biquad cell using two integrators [14]. Since the biquad cell is a key building block in any filter design, our method can be easily extended to higher order active filter designs. Compared to recently published active filter optimization work via GP in [15], our work focusses on presenting new modeling and optimization techniques that enable a fully-optimized transistor-level filter design, while the work in [15] emphasizes more on high-level design explorations with no actual circuit-level simulations/verifications.

Applying GP-based circuit optimization to the active filter design entails several inherent challenges. In this work, we focus on addressing two such challenges: 1) finding optimal biasing for individual transistors and 2) including modeling constraints that are not natively compatible with GP. In 1), conventional GP-based optimization assumes that transistors in a circuit are in the saturation region [10]. While this is a reasonable assumption in most cases, biasing transistors at the subthreshold region can often lead to significant power reduction due to high g_m/I_D which is transconductor efficiency. Transistors in the subthreshold region exhibit lower f_T compared with those in the saturation region; however, low f_T in the nanometer CMOS process can still be beyond multi-GHz, which is acceptable for many existing RF systems. At the same time, biasing every transistor at the subthreshold region in a given circuit structure would not necessarily yield a globally-optimal design. In this work, we embed a g_m/I_D-based selection algorithm in the GP-optimization so that a proper device operating region can be automatically and individually selected for transistors in a given circuit structure. This method helps improve the accuracy of the optimized design when low-power dissipation is the critical design metric. In 2), GP-based optimization requires that the circuit models must fit into specific functional forms, known as *posynoimal inequality* and *monomial equality*. For the active filter optimization, a key noise model equation is fundamentally not in posynomial form, which in general can't be handled via GP. To address this issue, we propose a designer-guided iterative method via a bisection algorithm, thereby including non-posynomial functions in the circuit models. While demonstrated only for noise model constraint in this work, the presented technique is general and therefore can be extended to handle other non-posynomial models in GP-based circuit optimization.

This paper is organized as follows. GP-based optimization is reviewed in Sect. 2. Section 3 presents active filter modeling for GP optimization. The target application of our filter design is low-energy RF transceivers, such as Bluetooth LE and IEEE 802.15.4q. Section 4 describes the proposed g_m/I_D-based selection algorithm and bisection algorithm to incorporate the non-posynomial model.

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Numerical results are shown in Sect. 5. Section 6 concludes the paper with a brief summary.

2. Review of GP-Based Optimization

Geometric programming is an optimization problem that can be transformed into a convex problem. Being a global optimization, an initial value for the solution is not necessary to find a globally optimal solution. Two types of functions are used in GP, namely *monomial* and *posynomial* functions. They have the following forms

$$f(x_1, x_2, \cdots, x_n) = \sum_{k=1}^{K} c_k x_1^{\alpha_{1k}} x_2^{\alpha_{2k}} \cdots x_2^{\alpha_{nk}} \tag{1}$$

where $c_k \geqq 0$ and $\alpha_{nk} \in \mathbf{R}$. When $K = 1$, f is called a monomial function; otherwise, f is a posynomial function, which essentially is a sum of the monomial functions. GP is an optimization problem that has a posynomial objective function of design variables x_i with a set of posynomial inequality constraints and monomial equality constraints:

$$\text{minimize} \quad f_0(x) \tag{2}$$

$$\text{subject to} \quad f_i(x) \leq 1, \quad i = 1, \cdots, m \tag{3}$$

$$g_i(x) = 1, \quad i = 1, \cdots, p \tag{4}$$

$$x_i > 0, \quad i = 1, \cdots, n. \tag{5}$$

By the logarithmic transformation of both variable x_i in (5) and the constraint and objective functions in (2), and (3)~(4), the GP problem can be solved as a convex programming problem; therefore, it can be efficiently solved using an interior point method [16]. Note that the obtained solution is guaranteed to be globally optimum due to the fundamental nature of convex optimization.

Table 1 shows several characteristics of various optimization methods for comparison of GP and other optimization techniques. The advantages of GP are its shorter optimization time and the availability of transistor-level and high-level optimization. Despite the high modeling effort required, GP has the significant advantage that it can analyze various design tradeoffs, as shown in Sect. 5.

Table 1 Several characteristics of various optimization methods.

	This work	[3]	[6]	[8]	[15]
Method	Geometric Programming	Genetic algorithm	General matrix-based approach	Numerical optimization	Geometric Programming
High-level Optimization	O	O	O	O	O
Transistor-level Optimization	O	X	X	X	O
Optimization Time	Fast	Fast	Normal	Slow	Fast
Design Tradeoff Analysis	Easy	Hard	Easy	Hard	Easy
Modeling effort	High	Normal	High	low	High

3. Active Filter Modeling

3.1 Device Modeling

To build a circuit model in a GP-compatible way, a process-dependent device model is needed. We create either monomial or posynomial functions of small signal parameters and bias voltages based on a convex piecewise-linear function fitting [17]. Data points obtained from DC sweep simulations in the foundry 65 nm-CMOS process are used. To assess the feasibility of including the subthreshold region into GP optimization, we generated both saturation and subthreshold mode models. The resulting device models are listed in Appendix. Table 2 shows mean/max percentage fitting errors ($|(y_{GPmodel} - y_{simul})/y_{simul}| \cdot 100$) of the key device models. The device models are functions of width W, length L, drain current I_{DS}, and V_{DS}. The range of the sweep simulation for L and V_{DS} are from 60 nm to 2 μm and from 50 mV to 350 mV, respectively. We assume a multi-finger transistor structure with a fixed finger width W = 120 nm. The comparison in Table 2 reveals that although the subthreshold model has a slightly higher modeling error due to its inherent exponential I_D-V_{GS} behavior, the model still shows reasonably good accuracy, leading us to conclude that including the subthreshold model into the GP optimization would not significantly degrade the quality of the

Table 2 Mean/Max % modeling errors in NMOS devices.

	Conventional device model in saturation	New device model in subthreshold
g_m_mon. (%)	3.8 / 7.2	5.4 / 11.7
$1/g_m$_posy. (%)	0.7 / 1.1	1.6 / 4.4
g_{ds}_mon. (%)	6.9 / 16.6	13.2 / 26.3
g_{ds}_posy. (%)	3.4 / 6.7	3.3 / 7.8
V_{GS}_mon. (%)	2.9 / 7.1	7 / 19.3
V_{GS}_posy. (%)	1.7 / 3.1	4.9 / 10.3
V_{TH}_mon. (%)	0.7 / 1	0.7 / 1.2
V_{DSAT}_mon. (%)	2.6 / 5	7.3 / 15.1
C_{gs}_mon. (%)	1.9 / 3.9	6 / 15.7
C_{js}_mon. (%)	0.0 / 0.04	0.01 / 0.02

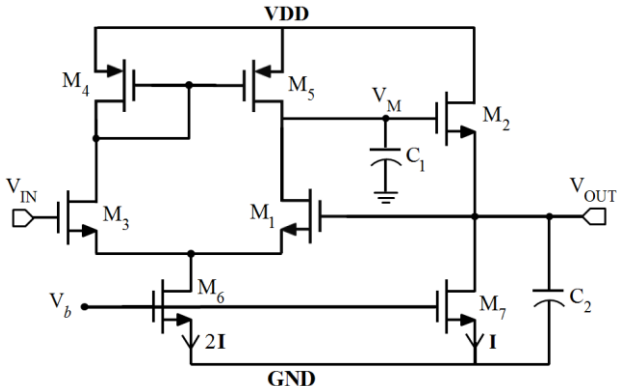

Fig. 1 Second-order active filter schematic.

optimization result. The design optimization method to select the proper operational region is presented in Sect. 4.

3.2 Circuit Modeling

The specific active filter we consider is shown in Fig. 1. The filter is essentially a cascade of two Gm-C stages with feedback to yield a single-ended biquadratic output. The first stage is a differential pair with an active current mirror followed by a source follower in the second stage. Our target application is a Bluetooth low-energy system where minimum energy is the most critical design goal.

1) Bias Model: To keep short channel devices in saturation, the following posynomial inequality is required:

$$(V_{DSAT} + \Delta V_{DSAT,min}) \cdot V_{DS}^{-1} \leq 1 \tag{6}$$

where $\Delta V_{DSAT,min}$ is the preset margin to prevent devices from operation in the triode region. A $\Delta V_{DSAT,min}$ of 10 mV is used in this design optimization. We impose (6) for every transistor in Fig. 1. With V_{DSAT} being a model parameter in Table 2, (6) is a posynomial inequality with a design variable V_{DS}.

We also impose an upper bound on the current efficiency as a posynomial inequality as

$$g_m \cdot I_{DS}^{-1} \cdot \eta_{max}^{-1} \leq 1 \tag{7}$$

p where η_{max} is the maximum current efficiency or $(g_m/I_{DS})_{\max}$. In modern processes, η_{max} is typically around 25 which is limited by g_m/I_{DS} in subthreshold region. In our model, we used $\eta_{max} = 35$ to explicitly detect the devices that are only limited by g_m/I_{DS} condition. As presented later in this paper, constraint (7) is used as a criterion in selecting devices in the subthreshold mode.

The matching constraints of a differential topology are modeled by the following five monomial equalities:

$$W_1 = W_3,\ L_1 = L_3,\ W_4 = W_5,\ L_4 = L_5,\ L_6 = L_7 \tag{8}$$

where W and L of each transistor are variables of the design optimization.

The circuit topology shown in Fig. 1 specifies Kirchhoff's current law (KCL) and Kirchhoff's voltage law (KVL) for node voltage and branch current, respectively, as

$$2 \cdot I_{DS1,3,4,5} = I_{DS6},\ I_{DS2} = I_{DS7} \tag{9}$$

$$|V_{GS4}| + V_{DS3} + V_{DS6} \leq V_{DD},\ V_{GS3} + V_{DS6} \leq V_{IN,CM} \tag{10}$$

$$V_{DS2} + V_{DS7} \leq V_{DD} \tag{11}$$

$$|V_{DS5}| + V_{GS2} + V_{GS1} + V_{DS6} \leq V_{DD} \tag{12}$$

where $V_{IN,CM}$ is the input common mode at the gate of M_3. KCL and current mirrors are expressed in (9). Inequality (10) constrains the bias voltage of the differential pair by KVL, and inequality (11) constrains the possible range of the drain-source voltages for M_2 and M_7. Inequality (12) is a critical constraint that includes four bias voltages within V_{DD}. In this paper, we use $V_{DD} = 0.6$V to reduce power dissipation. Therefore, with two gate-source voltages between the rails, the bias constraint in (12) is hard to satisfy. To reliably find a feasible bias condition and avoid potential current mismatch between I_{D4} and I_{D5} in the steady state, we impose extra bias constraints as

$$V_{GS5} \leq V_{GS5\_max},\ V_{DSAT5} \leq V_{DSAT5\_max} \tag{13}$$

where a V_{GS5_max} of 250 mV and a V_{DSAT5_max} of 100 mV are used in this optimization. These constraints guarantee that M_5 stays away from the triode region with a sufficient voltage margin.

2) Gain and Bandwidth Model: The second-order filter we consider in Fig. 1 has two poles within the feedback loop. The resulting closed-loop biquadratic transfer function can be modeled using quality factor Q and peaking frequency f_n. When open-loop transfer function $H(s)|_{open}$ is given by

$$H(s)|_{open} = \frac{A_v}{(1 + s/\omega_1)(1 + s/\omega_2)} \tag{14}$$

where A_v is the DC gain and ω_1 and ω_2 are pole frequencies, the closed-loop transfer function can be expressed as

$$\begin{aligned} H(s)|_{closed} &= \frac{H(s)|_{open}}{1 + H(s)|_{open}} \\ &= \frac{\omega_1\omega_2 A_v}{s^2 + (\omega_1 + \omega_2)s + \omega_1\omega_2 + \omega_1\omega_2 A_v}. \end{aligned} \tag{15}$$

One can easily show that f_n and Q in (15) are expressed as

$$f_n = \sqrt{\omega_1\omega_2 + \omega_1\omega_2 A_v}/2\pi \tag{16}$$

$$Q = \omega_n/(\omega_1 + \omega_2) \tag{17}$$

The A_v, ω_1, and ω_2 of the filter circuit shown in Fig. 1 can be found as

$$A_v = g_{m1,3}/(g_{ds1} + g_{ds5}) \tag{18}$$

$$\omega_1 = (g_{ds1} + g_{ds5})/C_M,\ \omega_2 = (g_{m2} + g_{ds7})/C_{OUT} \tag{19}$$

where C_M and C_{OUT} are the total capacitors at the M and output nodes, respectively,

$$C_M = C_1 + C_{gd1} + C_{gd2} + C_{gd5} + C_{jd1} + C_{jd5} \tag{20}$$

$$\begin{aligned} C_{OUT} = {} & C_2 + C_{gs1} + (1 + g_{m1}r_{O1})C_{gd1} + C_{gd7} \\ & + C_{js2} + C_{jd7}. \end{aligned} \tag{21}$$

By combining (20) and (21) with (16) and (17), one can express f_n and Q as

$$f_n = \sqrt{(g_{m1}+g_{ds1}+g_{ds5})(g_{m2}+g_{ds7})/4\pi^2 C_M C_{OUT}} \quad (22)$$

$$Q = \frac{\sqrt{(g_{m1}+g_{ds1}+g_{ds5})(g_{m2}+g_{ds7})/C_M C_{OUT}}}{(g_{ds1}+g_{ds5})/C_M+(g_{m2}+g_{ds7})/C_{OUT}}. \quad (23)$$

When Q is reasonably high, the gain at the peaking frequency can be approximated as the product of the closed loop DC gain $A_{v,closed}$ and the quality factor Q as

$$Gain = A_{v,closed} \cdot Q \quad (24)$$

where $A_{v,closed} \approx 1$ with unity-gain feedback in Fig. 1. Thus, if we choose the peaking frequency as the signal frequency, Q in (23) becomes simply the gain at the signal frequency. To impose gain and bandwidth constraints, we make a few approximations as

$$g_{m1} \gg g_{ds1,5},\ g_{m2} \gg g_{ds7},\ C_M \approx C_1,\ C_{OUT} \approx C_2. \quad (25)$$

With (25), the inverse of (22) and (23) squared can be used in posynomial inequalities as

$$\frac{f_{n,min}^2}{f_n^2} = f_{n,min}^2 \cdot \frac{(2\pi)^2 C_M C_{OUT}}{g_{m1} g_{m2}} \le 1 \quad (26)$$

$$\frac{Gain_{min}^2}{Gain^2} = Gain_{min}^2 \cdot \frac{\{C_M(g_{m2}+g_{ds7})+C_{OUT}(g_{ds1}+g_{ds5})\}^2}{C_1 C_2 g_{m1} g_{m2}} \le 1 \quad (27)$$

where $f_{n,min}$ and $Gain_{min}$ are lower bounds that are used in setting the specifications of the design optimization.

3) Noise Model: Noise performance is a key performance specification in any filter design. The total integrated noise power at output in a second-order system can be expressed for a given bandwidth and quality factors [18] as

$$P_{noise,out} = V_{n,0}^2 \cdot \frac{\pi}{2} \cdot f_n \cdot Q \quad (28)$$

where $V_{n,0}$ is the DC noise power spectral density at input. In our filter circuit in Fig. 1, $V_{n,0}$ is given by

$$V_{n,0}^2 = 4kT\gamma(g_{m3}+g_{m4})/{g_{m3}}^2 + 4kT\gamma(g_{m1}+g_{m5})/{g_{m1}}^2 \quad (29)$$

where noise factor γ is a thermal noise coefficient of the transistor. Ideally, γ has a value of 2/3, but it has been reported that experimental measurements show $\gamma \approx 1$ in a submicron CMOS process and γ depends also on channel length and bias voltage [19]. In our optimization, we consider such effects by creating a monomial model of γ as a function of L and IDS/W as

$$\gamma = a \cdot L^b \cdot (I_{DS}/W)^c = 0.7656 \cdot L^{-0.0063} \cdot (I_{DS}/W)^{0.0312} \quad (30)$$

which is generated by noise sweep simulations and model fitting in a foundry 65nm CMOS technology. The modeling error of γ is less than 8%. This approach enables us to optimize the noise performance of the filter while considering the dependence of γ on channel length and bias voltage.

Signal-to-noise ratio (SNR) at the filter output can be constrained as

$$SNR_{out,min} \le SNR_{out} = P_{sig,out}/P_{noise,out} \quad (31)$$

$$P_{sig,out} = A_{v,closed}^2 \cdot V_{in,peak}^2/2 \quad (32)$$

where $\mathrm{SNR}_{out,min}$ and $\mathrm{V}_{in,peak}$ can be determined from design specifications according to the applications. In our case, we assume that this filter is used as part of the image rejection filter in a Bluetooth low energy (LE) receiver. Bluetooth LE specifies the input sensitivity of −90 dBm and a bit error rate (BER) of 0.1%. To achieve a BER of 0.1% in the Gaussian minimum shift keying (GMSK) modulation scheme, an SNR of 10 dB is required in view of the total system. In this paper, we assume that an $\mathrm{SNR}_{out,min}$ of 15 dB is required at the filter block. Considering an input sensitivity of −90 dBm with receiver blocks before a filter, such as low-noise amplifier (LNA), an IQ generator, and buffer of the mixer, we can determine the magnitude of $\mathrm{V}_{in,peak}$. In this paper, we use $\mathrm{V}_{in,peak} = 1.26$ mV considering an LNA gain of 27 dB, an IQ generator gain of 3 dB, and a buffer gain of 12 dB. By combining the SNR constraint and noise equations, one can impose the overall SNR constraint as

$$\frac{2 \cdot SNR_{out,min}}{V_{in,peak}^2 \cdot 4}\left\{\frac{4kT\gamma(g_{m3}+g_{m4})}{{g_{m3}}^2} + \frac{4kT\gamma(g_{m1}+g_{m5})}{{g_{m1}}^2}\right\} \times \frac{g_{m2}(g_{m1}+g_{ds1}+g_{ds5})}{g_{m2}C_1 + (g_{ds1}+g_{ds5})C_2} \le 1 \quad (33)$$

which is *not* a posynomial inequality since the denominator has multiple terms. An algorithm to address this issue is presented later in Sect. 4.

4) Other Constraints: There are several other important design constraints that in general need to be included in active filter designs. These are not included in our model but can be added if the design specification changes.

- Stability: Phase margin of the feedback amplifier is directly related to the quality factor of the closed-loop system. Therefore, to specify certain phase margins, we can impose an upper bound on the quality factor.
- Linearity: Imposing active filter nonlinearity in a GP-compatible form is not straightforward, but one can indirectly specify the output linearity constraint of the filter by imposing a lower bound on the open-loop gain of the feed-forward amplifier [20].
- Area: Since the area of the filter is dominated by transistors and capacitors, area constraints can be expressed as a posynomial function as

$$A = k \cdot \left(\sum_{i=1}^{n} W_i \cdot L_i + C_{cap}/C_0\right) \quad (34)$$

where the sum of width-length products of transistors is

the total active area, C_{cap} is the total metal capacitance value, and C_0 is the capacitance value per unit area. k is an experimental fuzzy factor to include signal and supply routing overhead in an actual layout.

- Signal Swing: Headroom constraint can be modeled by adding extra term V_{swing} to (10)-(12) in the bias model. Since the output voltage swing of the filter is very small in our case, we do not have V_{swing} in the model. As described earlier in Sect. 3, the voltage swing is 1.26 mV at the filter output in our case, which can be neglected in the design optimization.

4. Device Selection/Bisection Method

4.1 Subthreshold Device Selection

As discussed earlier in the paper, biasing transistors in the subthreshold region can lead to significant power benefits. Since all transistors need not operate in the subthreshold region, the algorithm should selectively choose optimal biasing for each transistor individually. Figure 2 shows our two-step subthreshold device selection algorithm. For the convenience of discussion, type-A devices use the device models extracted for the saturation mode, while type-B is the one for the subthreshold mode. As a first-pass optimization, we begin nominal GP optimization assuming all devices are type-A. To find out which devices are required to be replaced by a type-B model, we check the current efficiency g_m/I_{DS} of every transistor obtained from the first-pass optimization. If the upper bound imposed on g_m/I_{DS} in (7) turns out to be active for a certain transistor, we interpret this as an indication that biasing the particular transistor at the subthreshold region can lead to improvement in the optimization result. After substituting such devices with the type-B model, we perform second-pass optimization to obtain better optimal results using both type-A and type-B device models. This simple two-step approach significantly improves the accuracy of the optimization result, as shown later in this paper.

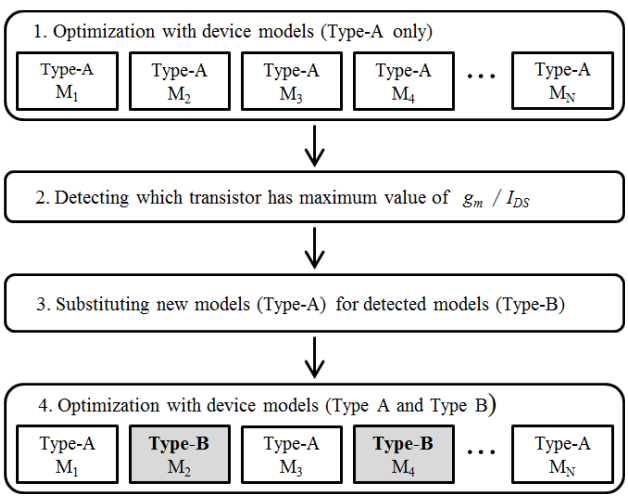

Fig. 2 Subthreshold device selection algorithm.

4.2 Bisection Method for Non-Posynomial Constraints

Non-posynomial constraints can occur in creating circuit models as exemplified in (33). A numerical technique is required to incorporate non-posynomial equations into a GP framework. We present a simple bisection method to address this issue, which is illustrated in Fig. 3. In our specific example, the problem in (33) is that the denominator terms

$$g_{m2}C_1 + (g_{ds1} + g_{ds5})C_2 \tag{35}$$

cannot be simply approximated as a monomial. To begin iteration, we first assume equal output conductance g_{ds1} and g_{ds5} to simplify (35) as $g_{m2}C_1 + 2g_{ds1}C_2$. Afterwards, we find the ratio between the two terms $g_{m2}C_1$ and $2g_{ds1}C_2$ through iterations using the bisection method, which is also known as the binary search method. To reach the final value within a reasonable number of iterations, a realistic range of the feasible ratio must be determined before the iteration begins. We note from the circuit structure in Fig. 1 that $g_{m2}C_1/2g_{ds1}C_2$ is essentially ω_2/ω_1 in (19), which is the ratio of two poles. We will refer to this term as *pole proximity*. Since the first pole ω_1 and the second pole ω_2 are located relatively close in this design optimization, we assume that the pole proximity $g_{m2}C_1/2g_{ds1}C_2$ may have a value between 0 and 2. The initial value of the pole proximity at the beginning of the algorithm is set at the middle of the feasible range. We then perform a series of GP optimizations to find the estimated optimal pole proximity value by narrowing down the search domain. In each iteration, the domain of the search is halved by comparing the pole proximity values from the optimization result and the estimated proximity value. Iteration is completed if the error from the comparison becomes less than 1%, which indicates the non-posynomial problem is solved properly.

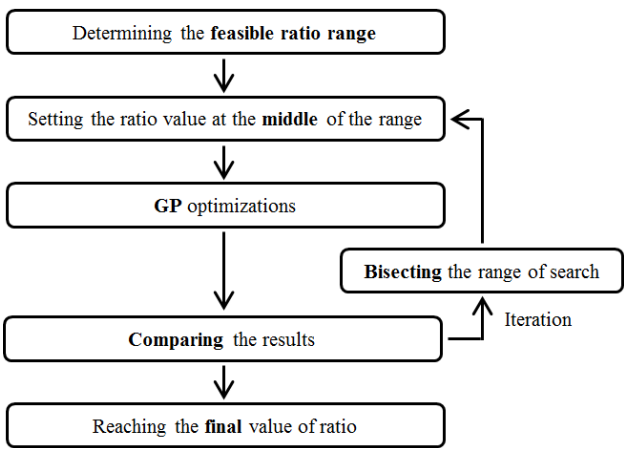

Fig. 3 Iterative optimization flow through bisection method.

5. Numerical Results and Discussion

5.1 Second-Order Filter Design Optimization

The Gm-C biquad shown in Fig. 1 is designed via GP-based optimization with the target design specification shown in Table 3. The resulting design was verified by Spectre simulations. Table 3 summarizes the comparison between the optimization results and the Spectre simulation. The specification of f_n is 2 MHz, which is the bandwidth of the low-pass filter with attenuation of 40 dB/decade. The SNR specification is 15 dB as required at the filter block from the system SNR budget. The actual optimization model is written and optimized using CVX, a convex optimization package for MATLAB [21]. For a given design specification, the optimized transistor-level filter consumes 0.62 μW. Errors between the optimization results and the simulation are less than 5% for all design specifications, indicating that the proposed GP-based optimization is performed with reasonably good accuracy.

To highlight the benefit of the optimal subthreshold/saturation mode selection, we compare the results from the first-pass (using the Type-A device in Fig. 2) and second-pass optimization (using Type-A and Type-B devices), as described in Sect. 4-A. It turns out that the second-pass optimization opts for the subthreshold mode for transistors M_1, M_2, and M_3. The comparison in Table 4 indicates that the modeling accuracy is considerably improved in the second-pass optimization; here, the error refers to the deviation between the optimization result and the Spectre simulation. Two data points at $f_n \geqq 1$ MHz and $f_n \geqq 2$ MHz are shown to compare the errors. As evident from Table 4, the errors from the first-pass optimization without the subthreshold mode device model are significantly higher than the second-pass optimization in all performance metrics, such as gain, f_n, and SNR. Table 4 also reveals that such errors are the direct consequence of the inaccuracy in estimating small-signal parameters, such as g_m and g_{ds}. On the other hand, the error in the small-signal parameters in the second-pass optimization result is reasonably small in all performance metrics. Therefore, it can be said that the proposed two-step subthreshold/saturation selection algorithm helps enhance the accuracy of optimization.

The feasibility of the bisection algorithm presented in Sect. 4-B has also been verified. Our target is to find an accurate final value of the term $(g_{m2}C_1/2g_{ds1}C_2)$ in (35). A graphical illustration using a numerical example is shown in Fig. 4. In the first iteration, the pole proximity value that we use in the optimization is 1 (denoted as a blue square). After the first-pass optimization, the actual proximity value obtained from the simulation is 0.56 (denoted as a red triangle), which is less than our estimated pole proximity value of 1. Since the actual value obtained from the optimization is lower than the middle of the feasible region, we update the expected pole proximity value to be in the middle of the lower bound of the feasible range (= 0) and the expected value used in the prior iteration (= 1), leading us to use 0.5 as the expected pole proximity value in the second-pass optimization. The sequential GP optimizations continue until both the expected value and the actual optimization result converge to a given error tolerance. In the case of our SNR optimization for the active filter design, the error becomes less than 1% when the number of iterations is beyond 7. By adopting this bisection method, the non-posynomial

Table 3 GP Optimization result and Simulation for proposed optimization.

Performance	Spec.	Optimization Result	Spectre Simulation	Error (%)
Power (μW)	Minimize	0.62	0.62	0
Gain (dB)	$\geqq$3	3	3.14	4.7
f_n (MHz)	$\geqq$2	2	1.97	–1.5
SNR (dB)	$\geqq$15	15	15.3	2

Table 4 Error between optimization result and spectre simulation.

	Error in first-pass optimization (%)		Error in second-pass optimization (%)	
	$f_n \geqq$ 1MHz	$f_n \geqq$ 2MHz	$f_n \geqq$ 1MHz	$f_n \geqq$ 2MHz
Gain	–24.9	–37.1	10.6	–11.3
f_n	–57.2	–76	–0.4	–8.2
SNR	31.7	99	–14.8	18.2
g_m (M_1)	–41	–41.3	0.9	–1.5
g_{ds} (M_1)	5.8	–4.4	3	–9.5
C_{gs} (M_1)	–10	–11	–0.5	–0.03
g_m (M_2)	–30.2	–28.8	16.5	13.5
g_{ds} (M_2)	–52.4	–45.8	–12	–13.4
C_{gs} (M_2)	–6	–10.3	–4.1	–2.4

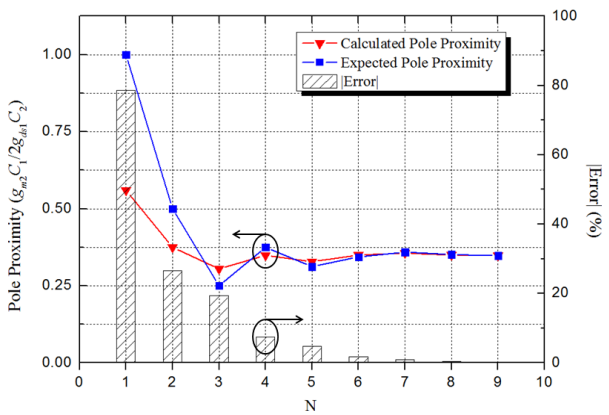

Fig. 4 Expected pole proximity and calculated pole proximity from optimization according to the number of iterations N through the bisection method and the absolute value of the error.

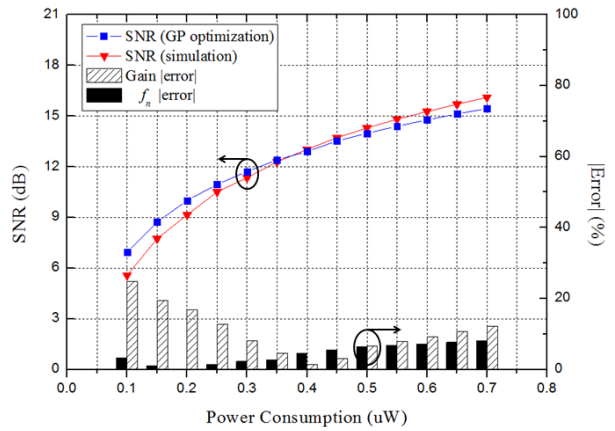

Fig. 5 SNR versus power consumption from GP optimization and the simulation and absolute value of the error between GP and the simulation for gain and f_n.

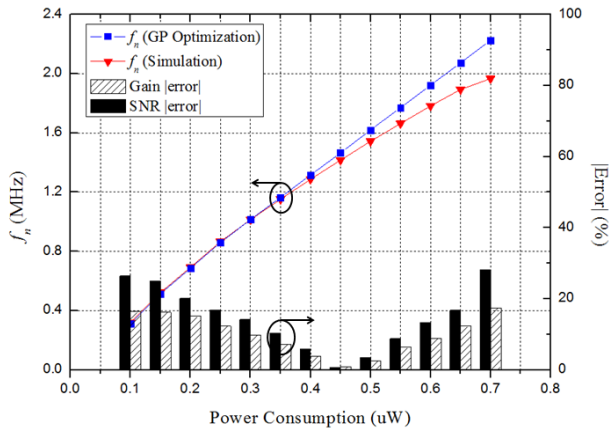

Fig. 6 f_n versus power consumption from the GP optimization and the simulation and the absolute value of the error between the GP and the simulation for gain and SNR.

constraint can be incorporated in the GP framework.

5.2 Power-Performance Tradeoff Analysis

Design optimization can provide useful power performance tradeoffs that can help guide system-level design optimization. For instance, Fig. 5 shows the GP optimization and simulation results of power dissipation while varying the SNR specification in the optimization. As the SNR requirement increases, it can be seen that the power consumption rises. It is interesting to note that the power cost to increase the SNR is mild when the SNR specification is less than 11 dB, while the power cost to increase the SNR becomes much larger when the SNR requirement exceeds 11 dB. Also, Fig. 5 reveals that the absolute values of the error between the simulation and the optimization at each data point indicate that our filter model has reasonably good accuracy. More specifically, average errors of the gain and f_n are 10.6% and 4.4%, respectively. The sensitivity of the total power on the SNR requirement can be leveraged to optimally assign power and noise budgets in the RF receiver design.

Another example of power-performance tradeoffs is shown in Fig. 6. Since f_n represents the bandwidth of the filter, Fig. 6 illustrates the power-bandwidth tradeoff. As the f_n requirement increases, it can also be seen that the power dissipation rises. Optimization accuracy is maintained at each data point. In this experiment, average errors of the gain and SNR are 9.9% and 14.6%, respectively, indicating a good numerical accuracy of the optimization model is maintained over wide ranges of design specifications.

Table 3 shows several characteristics of many optimization methods to compare GP and the other optimization technique. Advantages of GP are optimization time and availability of transistor level and high-level optimization. In spite of high modeling effort, GP has significant advantage that can analyze various design tradeoff as it is shown in Sect. 5.

6. Conclusions

In this paper, we proposed an active-filter optimization method via geometric programming. The presented equation-based active filter model along with new modeling techniques are shown to efficiently optimize a transistor-level active filter for a given design specification. The two-step selection method for choosing the saturation and subthreshold modes has been proposed to enhance the accuracy of the optimization result for low-power designs. A bisection method has been applied to incorporate non-posynomial constraints in the GP optimization. The numerical experiments to validate the proposed modeling techniques show that the optimized designs achieve good accuracy over wide ranges of design specifications. Additionally, our optimization method can efficiently explore the optimal power-performance tradeoffs of an active filter, which can be very useful in deciding the block-level power budget in an RF system design.

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Appendix:

In device modeling, either monomial or posynomial functions of small-signal parameters and bias voltages based on a convex piecewise-linear function fitting are created. Monomial models of several parameters in Table 2 are expressed as:

$$\begin{aligned}
\text{M1_gmmon} &= \text{M1_m} \cdot \alpha_1 \\
&\quad \cdot (\text{M1_l})^{\beta 1} (\text{M1_id})^{\gamma 1} (\text{M1_vds})^{\delta 1}, \\
\text{M1_gdsmon} &= \text{M1_m} \cdot \alpha_2 \\
&\quad \cdot (\text{M1_l})^{\beta 2} (\text{M1_id})^{\gamma 2} (\text{M1_vds})^{\delta 2}, \\
\text{M1_vgsmon} &= 1 \cdot \alpha_3 \cdot (\text{M1_l})^{\beta 3} (\text{M1_id})^{\gamma 3} (\text{M1_vds})^{\delta 3}, \\
\text{M1_vthmon} &= 1 \cdot \alpha_4 \cdot (\text{M1_l})^{\beta 4} (\text{M1_id})^{\gamma 4} (\text{M1_vds})^{\delta 4} \\
\text{M1_cgsmon} &= \text{M1_m} \cdot \alpha_5 \cdot (\text{M1_l})^{\beta 5} (\text{M1_id})^{\gamma 5} \\
\text{M4_gmmon} &= \text{M4_m} \cdot \alpha_6 \\
&\quad \cdot (\text{M4_l})^{\beta 6} (\text{M4_id})^{\gamma 6} (\text{M4_vds})^{\delta 6}, \\
\text{M4_gdsmon} &= \text{M4_m} \cdot \alpha_7 \\
&\quad \cdot (\text{M4_l})^{\beta 7} (\text{M4_id})^{\gamma 7} (\text{M4_vds})^{\delta 7}, \\
\text{M4_vgsmon} &= 1 \cdot \alpha_8 \cdot (\text{M4_l})^{\beta 8} (\text{M4_id})^{\gamma 8} (\text{M4_vds})^{\delta 8}, \\
\text{M4_vthmon} &= 1 \cdot \alpha_9 \cdot (\text{M4_l})^{\beta 9} (\text{M4_id})^{\gamma 9} (\text{M4_vds})^{\delta 9}, \\
\text{M4_cgsmon} &= \text{M4_m} \cdot \alpha_{10} \cdot (\text{M4_l})^{\beta 10} (\text{M4_id})^{\gamma 10}, \\
\text{M6_gmmon} &= \text{M6_m} \cdot \alpha_{11} \\
&\quad \cdot (\text{M6_l})^{\beta 11} (\text{M6_id})^{\gamma 11} (\text{M6_vds})^{\delta 11}, \\
\text{M6_gdsmon} &= \text{M6_m} \cdot \alpha_{12} \\
&\quad \cdot (\text{M6_l})^{\beta 12} (\text{M6_id})^{\gamma 12} (\text{M6_vds})^{\delta 12}, \\
\text{M6_vgsmon} &= 1 \cdot \alpha_{13} \cdot (\text{M6_l})^{\beta 13} (\text{M6_id})^{\gamma 13} (\text{M6_vds})^{\delta 13}, \\
\text{M6_vthmon} &= 1 \cdot \alpha_{14} \cdot (\text{M6_l})^{\beta 14} (\text{M6_id})^{\gamma 14} (\text{M6_vds})^{\delta 14}, \\
\text{M6_cgsmon} &= \text{M6_m} \cdot \alpha_{15} \cdot (\text{M6_l})^{\beta 15} (\text{M6_id})^{\gamma 15},
\end{aligned}$$

where $\alpha_1 = 5.56$, $\beta_1 = -0.023$, $\gamma_1 = 0.93$, $\delta_1 = 0.0095$, $\alpha_2 = 0.0043$, $\beta_2 = -0.26$, $\gamma_2 = 0.94$, $\delta_2 = -0.63$, $\alpha_3 = 8.19$, $\beta_3 = -0.053$, $\gamma_3 = 0.31$, $\delta_3 = -0.103$, $\alpha_4 = 0.0061$, $\beta_4 = -0.24$, $\gamma_4 = 2.88 \cdot 10^{-05}$, $\delta_4 = -0.033$, $\alpha_5 = 1.03 \cdot 10^{-07}$, $\beta_5 = 1.12$, $\gamma_5 = 0.17$, $\alpha_6 = 5.56$, $\beta_6 = -0.023$, $\gamma_6 = 0.93$, $\delta_6 = 0.0095$, $\alpha_7 = 0.0043$, $\beta_7 = -0.26$, $\gamma_7 = 0.94$, $\delta_7 = -0.63$, $\alpha_8 = 8.19$, $\beta_8 = -0.053$, $\gamma_8 = 0.31$, $\delta_8 = -0.103$, $\alpha_9 = 0.02$, $\beta_9 = -0.16$, $\gamma_9 = 5.09 \cdot 10^{-05}$, $\delta_9 = -0.0047$, $\alpha_{10} = 1.15 \cdot 10^{-08}$, $\beta_{10} = 1.06$, $\gamma_{10} = 0.082$, $\alpha_{11} = 0.0012$, $\beta_{11} = -0.3$, $\gamma_{11} = 0.64$, $\delta_{11} = 0.083$, $\alpha_{12} = 0.00035$, $\beta_{12} = -0.34$, $\gamma_{12} = 0.87$, $\delta_{12} = -0.85$, $\alpha_{13} = 34.27$, $\beta_{13} = 0.078$, $\gamma_{13} = 0.27$, $\delta_{13} = -0.069$, $\alpha_{14} = 0.0063$, $\beta_{14} = -0.23$, $\gamma_{14} = 0.001$, $\delta_{14} = -0.04$, $\alpha_{15} = 1.07 \cdot 10^{-08}$, $\beta_{15} = 1.06$, and $\gamma_{15} = 0.076$. Monomial models of M_1 are new device NMOS models in the subthreshold mode. Monomial models of M_4 and M_6 are PMOS and NMOS models, respectively, which are conventional device models in the saturation mode.

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