Measurement and analysis: Usually, an omni-directional radiation pattern is requested for an antenna used in the mobile communication terminal. To check whether a POD antenna may have such a feature, first an ITO strip forming a monopole with 38 mm length and 3 mm width is vertically installed on a 30 × 30 mm metal ground plane. By operating the antenna at 1.8 GHz, the radiation pattern with its vertical polarisation is measured and observed to be quite omni-directional. Therefore, this innovatory concept of antenna design offers the radiation characteristics of a common monopole antenna. As shown in the LCD display in Fig. 2, the GSM handset employing a POD antenna achieved full RF strength from the base station and operates very satisfactorily.

For purpose of comparison, another ITO trapezoid radiator, similar to that in Fig. 1 yet with top width 28 mm, down width 20 mm and height 20 mm, was also fabricated by a sputtering approach. At 1.8 GHz its measurement of the radiation pattern of vertical polarisation is shown in Fig. 3. The property of the omni-directional pattern is maintained.

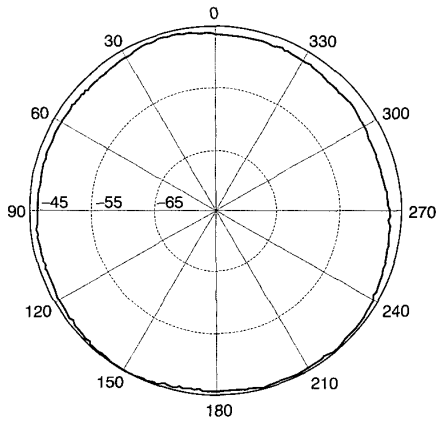

Fig. 3 *Radiation pattern generated by ITO radiator made by sputtering process*

Regarding the characteristics of input impedance, Fig. 4 shows the measured S_{11} parameter of the ITO radiator in Fig. 1. 1.8 GHz is chosen as the operating frequency in the radiation measurements since that is the RF carrier of the GSM system. This radiator has better resonant condition at around 2.2 GHz: even so, under the same measuring condition, it has been found that its maximum received directional power is 2.33 dB less compared with a normal 1.8 GHz GSM monopole antenna. Thus, the POD antenna is regarded as a good candidate for mobile terminals in wireless communication. However, for a better matching operation with the RF front-end of mobile terminals the ITO radiator should be further tuned up in shape or other configuration.

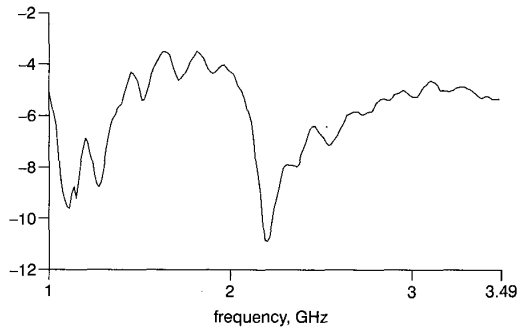

Fig. 4 *Measured $|S_{11}|$ of ITO radiator in Fig. 1*

Conclusion: An innovatory printed-on-display (POD) antenna is reported. The purposed this new type of antenna is to increase the product value of the LCD panel since it combines the antenna and display functions together as a hardware module.

Because of its embedding feature, the POD antenna is also suitable to be applied on a terminal which operates with multi-RF systems for multi-purposes at the same time, e.g. GSM plus GPS, GSM plus bluetooth and so forth. It may be applied for either one of these multi-functions.

The final goal of this proposal is to commercialise the POD antenna in the display industry; consequently, the electrical interface between the display unit and circuit board may be standardised to ensure a signal path for the POD antenna and the RF circuit on the board.

Acknowledgment: This present work is supported by the National Science Council of the Republic of China, grant NSC 89-2213-E-036-027.

20 May 2002
Electronics Letters Online No: 20020840
DOI: 10.1049/el:20020840

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Size reduction of microstrip antenna by elevating centre of patch

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A new structure of microstrip patch antenna with considerable reduction in its size and wide impedance bandwidth, with marginally degraded antenna performances, is proposed. These merits are obtained by elevating the centre of the radiating metallic patch, and thus increasing the electrical length of that patch more effectively. These, for purpose of example, the proposed size-reduced antenna has been designed and tested at 3 GHz and 53% of size reduction is achieved compared with the conventional one. It showed the possibility that the non-planar antenna structure can provide new design opportunity for compact devices.

Introduction: Microstrip antennas are the most common form of printed antennas and are used in a broad range of applications owing to their simplicity, conformal nature, low manufacturing cost, and easy analysis and design using several field simulators [1, 2]. However the size of microstrip antennas becomes too large for low frequency applications, especially for handheld devices since this antenna is a kind of resonant antenna. Several techniques have been previously demonstrated to reduce the size of the patch antenna, including: the use of high permittivity substrates; modifying the patch shape; and the use of shorting posts [3, 4]; and recent studies have proposed a corrugated patch antenna in order to overcome limitations of these size-reducing techniques [5]. However, the simple corrugation of the metallic patch without considering distributions of fields or currents on an antenna cannot reduce the antenna size dramatically. In this Letter we present a new patch shape with the properly located elevation so that it can maximise the effects of capacitance C and inductance L of the patch on the size reduction of a conventional planar patch antenna much more than the corrugated patch antenna. Through this new type of design, the reduction of antenna length by at least 50% for a given resonant frequency is possible.

Proposed antenna: The proposed antenna structure is shown in Fig. 1. The discontinuity of the height of the radiating metallic acts as an inductive load in series with an equivalent transmission line and reduces the effective phase velocity of the propagating wave. Moreover, this patch with an elevation on its centre (see Fig. 2) increases the electrical length of the antenna more effectively than a simply

corrugated one since electric currents are maximum on the centre of the patch. Also, it does not reduce the capacitance of the patch since the height is unchanged on both sides of patch and they are the main contributor of the capacitance of the patch. The resonant frequency of the antenna is found to be decreased with an increase in elevation height H.

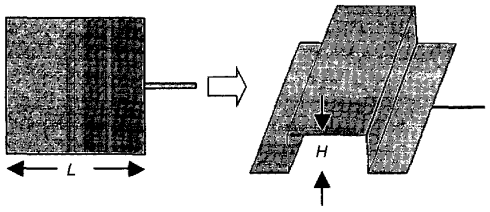

Fig. 1 *Antenna dimension reduction*

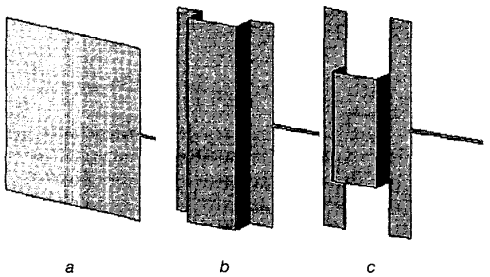

Fig. 2 *Antennas*
a Conventional square patch
b Patch with elevation on centre
c As *b* with additional notch

Results: To verify the effects of the proposed shape of patch on the size reduction and performances of antenna, input return loss and radiation patterns are simulated and measured, and then compared to the conventional planar patch antenna. In designs, the substrate of dielectric constant 2.2 and thickness 0.7874 mm is used, and the length L of baseline patch antenna is 32.65 mm, which is resonant length at 3 GHz. And, for convenience, the elevation height H for the case of elevated patch is fixed by the value of a quarter of the patch length. Moreover, the elevated patch antenna with an additional notch (discontinuity in patch width) on its centre is also designed for comparison. The measured performances of these different types of antennas resonant at 3 GHz are compared and summarized in Fig. 2. As shown in Fig. 2 and Fig. 3, compared with the reference structure, the (type *b*) elevated patch antenna has wide impedance bandwidth with considerably reduced antenna length at the expense of the antenna gain. Also, comparing with the corrugated patch, we can see that considerable reduction of the patch size is possible only by elevating the centre of patch. Fig. 4 shows the measured radiation patterns of the antenna. Although the (type *c*) elevated patch antenna with notch can reduce the antenna length even more, this type of antenna has degraded impedance and gain characteristic due to the radiation from the edges of notch [3, 4]. Almost identical beam pattern with a conventional one is obtained along the H-plane and a more broadened pattern is obtained along the E-plane as expected. Some deviations from simulated results near the horizon can be thought to be due to the finite ground effect.

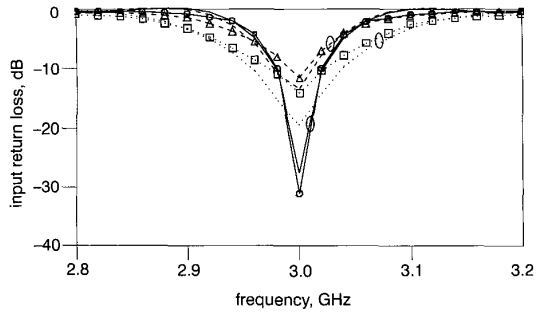

Fig. 3 *Input return losses*
——— conventional square patch, simulated
—○— conventional square patch, measured
– – – – – patch with elevation on centre, simulated
– – –□– – – patch with elevation on centre, measured
— — — — as *b* of Fig. 2 with additional notch, simulated
— — △ — — as *b* of Fig. 2 with additional notch, measured

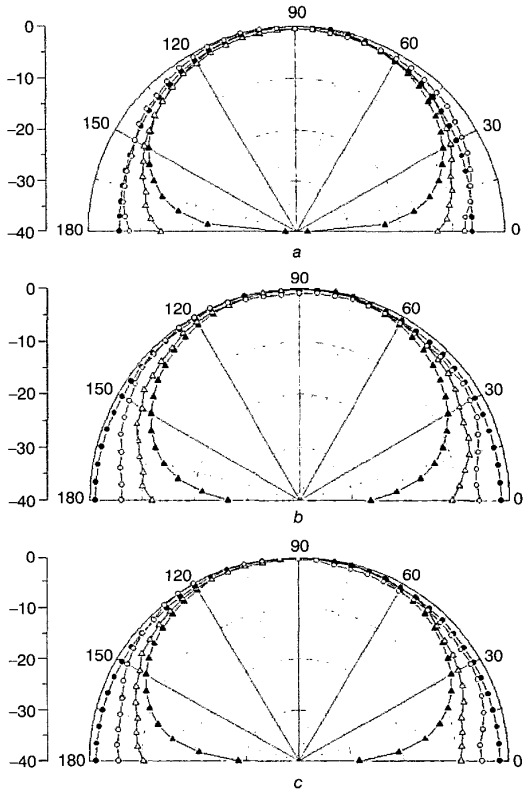

Fig. 4 *Antenna radiation patterns*
a Conventional square patch
b Patch with elevation on centre
c As *b* with additional notch
——●—— *E*-plane patterns, simulated
– – – ○ – – – *E*-plane patterns, measured
——▲—— *H*-plane patterns, simulated
– – – △ — *H*-plane patterns, measured

Table 1: Comparisons of measured antenna performances

Performances	Conventional	Elevation on centre	With additional notch
−10 dB bandwidth (%)	1.37	1.96	0.70
3 dB beamwidth (deg)			
E-plane	100	130	135
H-plane	85	90	92
Gain (dBi)	4.1	3.1	2.6
Length reduction (%)	–	53	64

Conclusions: A new structure of the size-reduced patch antenna with marginally degraded antenna performances is proposed. By using the elevation on its centre of the patch, we can reduce the length of conventional square patch antenna by more than 50%. This implies that simple corrugation for increasing the electrical length of the patch has a limit to size reduction of patch antennas. Also, these results suggest that non-planar antenna structures may offer new design opportunities for low-cost compact devices.

Acknowledgment: This work was supported by KOSEF under the ERC program through the MINT research centre at Dongguk University.

21 June 2002
Electronics Letters Online No: 20020798
DOI: 10.1049/el:20020798

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Current-mode fully-programmable piece-wise-linear block for neuro-fuzzy applications

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A new method to implement an arbitrary piece-wise-linear characteristic in current mode is presented. Each of the breaking points and each slope is separately controllable. As an example a block that implements an N-shaped piece-wise-linearity has been designed. The N-shaped block operates in the subthreshold region and uses only ten transistors. These characteristics make it especially suitable for large arrays of neuro-fuzzy systems where the number of transistors and power consumption per cell is an important concern. A prototype of this block has been fabricated in a 0.35 μm CMOS technology. The functionality and programmability of this circuit has been verified through experimental results.

Introduction: A piece-wise-linear element is commonly required to implement the activation function of neural systems and the membership function in the case of fuzzy systems [1]. In most cases, complete programmability of the breaking points and slopes of the different pieces of the nonlinearity is desirable. Normally, it is necessary to implement an activation (or membership) function per neural (or fuzzy) cell. The large number of cells integrated in VLSI neural and fuzzy systems make the simplicity (in transistor number) and power consumption of the piece-wise-linear block important concerns.

In the following Section, a new method to implement a current-mode piece-wise-linear characteristics is presented. A block implementing an N-shaped piece-wise-linearity is then introduced. The block requires only ten transistors per cell and can be operated at very wide current ranges. A small prototype has been fabricated in a CMOS 0.35 μm technology. Experimental results are provided.

Current-mode piece-wise-linear block: Any arbitrary unidimensional piece-wise-linear function $f(u)$ can always be decomposed as the sum of one-sided rectified functions:

$$f(u) = \sum_i (\pm m_i[\pm(u - u_i)]^+) \quad (1)$$

where $[x]^+$ denotes the one-sided rectification operator (x if $x \geq 0$ or 0 if $x \leq 0$), m_i is the slope of the gain segment and u_i is its breaking point. Fig. 1*a* shows the four possible one-sided rectified functions which correspond to the two possible signs of the slope and the two possible signs of the output function. Each sub-figure in Fig. 1*b* shows a proposed current-mode circuit block that implements each of the functions in Fig. 1*a*. The transistors in Fig. 1*b* are intended to operate in the subthreshold region. This way, the slopes m_i of the gain segments can be controlled through the bias voltages V_{ia} and V_{ib}. In particular,

$$m_i = \exp\left(\frac{V_{ia} - V_{ib}}{nU_T}\right) \quad (2)$$

where n is the slope factor of the MOS transistors (NMOS n_n or PMOS n_p) in the subthreshold region [2]. However, the large variability of the slope factors (n_n, n_p) and the transistor threshold voltages (V_{Tn}, V_{Tp}) from run to run, makes it impractical to control the m_i slopes by controlling directly the voltage biases. This inconvenience can be solved using current biases to control the slopes. Fig. 2 shows the NMOS and PMOS versions of the biasing blocks. The current references u_{ref} and $m_i u_{ref}$ are used to set the appropriate values of the voltages V_{ia} and V_{ib}, such that the ratio between the currents flowing through the two branches is m_i. In a large neural or fuzzy system, the biasing blocks are common to all the cells in the chip. The amplifiers in Fig. 2 must deliver sufficient current to all the output branches in the different cells. This means that the output stage of the amplifiers must be scaled with the number of cells in the chip.

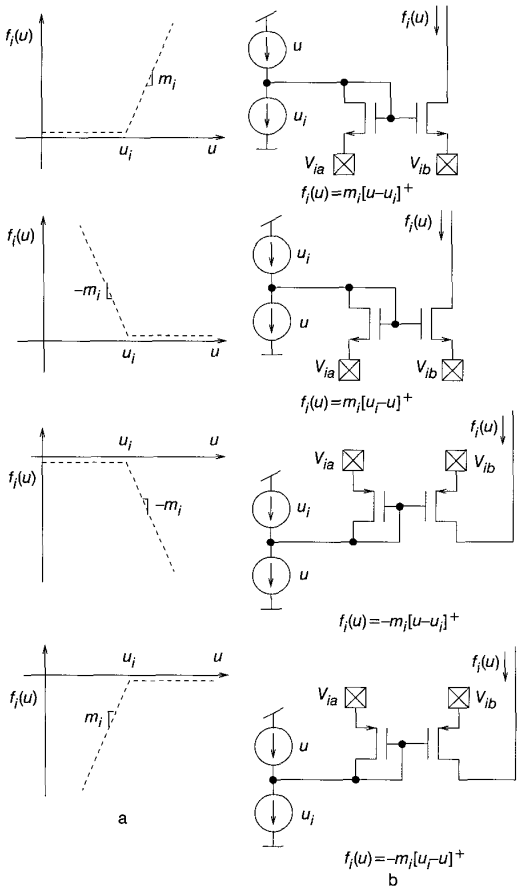

Fig. 1 *Functions and implementations*
a Four possible one-sided rectified functions
b Schematic of four implementations

In our application, we needed to synthesise an N-shaped PWL function such as that shown in Fig. 3, which is a block commonly used as the activation function in neural networks implementations. The block must be adaptive, i.e. we want to control independently the two breaking points u_1, u_2 and the three slopes m_0, m_1 and m_2. As shown in Fig. 3, the PWL function $f(u)$ can be decomposed as the sum of three components, named as $f_0(u)$, $f_1(u)$ and $f_2(u)$ in Fig. 3. Fig. 4 shows the schematics of the current-mode block synthesised using our general method explained so far. The proposed method is generic for any piece-