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Design of lowpass filters using defected ground structure and compensated microstrip line

Jong-Sik Lim, Chul-Soo Kim, Young-Taek Lee, Dal Ahn and Sangwook Nam

A method to design lowpass filters (LPF) using defected ground structure (DGS) and compensated microstrip line is presented. Using the extracted equivalent elements of DGS and capacitive microstrip line, an LPF having no open stub, high impedance line, and tee- or cross-junction element, is designed. Only two DGS patterns and one broad microstrip line comprise the LPF. Simple structure, small size (half of a conventional LPF), less discontinuities, and high power handling capability are obtained through the proposed LPF.

Introduction: It is well known that periodic structures typically have lowpass characteristics. The widely used periodic structures for microstrip lines are various kinds of photonic bandgap (PBG) [1–3] and defected ground structure (DGS) [4]. DGS is realised by etching off a defected pattern from the ground plane. In this Letter, DGS is composed of two square defected areas and a narrow connecting slot. These are the sources of the equivalent L-C elements. DGS has simple structure, equivalent circuit elements, and potentially great applicability to design couplers, dividers and amplifiers [5–7].

Conventional microstrip lowpass filters (LPFs) have deep low-high impedance lines and serious discontinuities between them, or open stubs connected to junction elements. To remove these disadvantages, a method that uses only two DGS patterns and one compensated microstrip line to design LPFs is discussed. There are no open stubs, high impedance lines, and junction elements such as tee and cross in the proposed LPF.

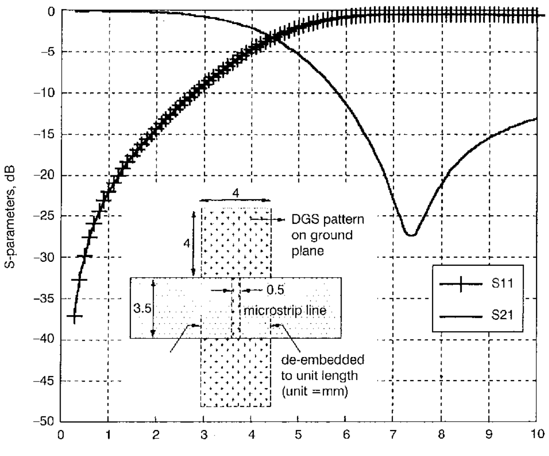

Fig. 1 *Microstrip line having dumb-bell-shaped DGS pattern and characteristics by EM simulation ($\varepsilon_r = 3.48$, thickness = 30 mils)*

DGS pattern and equivalent circuit: Fig. 1 shows a microstrip line with dumb-bell-shaped DGS and predicted performances by electromagnetic (EM) simulation. The square-type defect can be replaced by circle- or octagon-shape. It is intuitively understood that there are equivalent L-C elements, as shown in Fig. 2*a*, due to the resonant and 3 dB cutoff frequencies. Since the same properties can be seen from the one-pole Butterworth prototype LPF, Fig. 2*b* is the equivalent to Fig. 2*a*. Because reactances are expressed as (1) and (2), the equality at cutoff frequency should be preserved by (3):

$$X_{LC} = \frac{1}{\omega_o C((\omega_o/\omega) - (\omega/\omega_o))} \tag{1}$$

$$X_L = \omega' Z_o g_1 \tag{2}$$

$$X_{LC}|_{\omega=\omega_o} = X_L|_{\omega'=1} \tag{3}$$

where ω_o, ω', g_1 and Z_o are the resonant frequency, normalised cutoff frequency, prototype value of the Butterworth-type LPF, and the scaled port impedance, respectively.

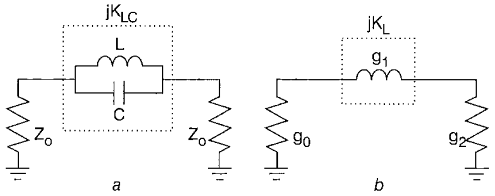

Fig. 2 *Equivalent circuit of microstrip line with unit DGS, and Butterworth prototype of one-pole LPF*

a Microstrip line with unit DGS
b Butterworth prototype

The extracted L and C are 2.2832 nH and 0.2026 pF. Fig. 3 shows the predicted characteristics of the parallel L-C network on a circuit simulator with the EM simulation results overlapped.

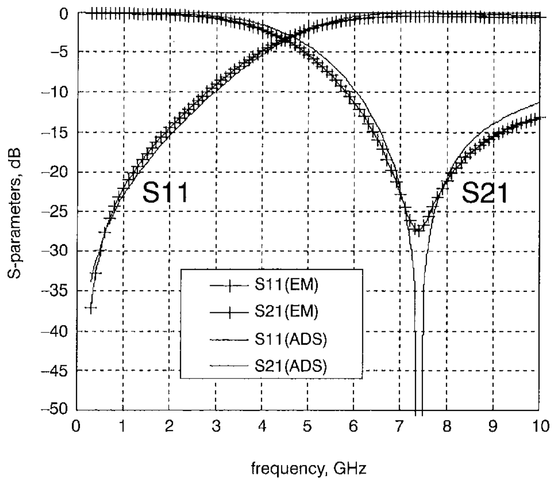

Fig. 3 *Characteristics of L-C network with EM simulation results overlapped*

Design of microstrip LPF using DGS: An LPF with 0.01 dB ripple was designed using two L-C resonators and one shunt capacitor as shown in Fig. 4*a*. This is a typical topology of an LPF. L1, C1, and C2 are 2.2832 nH, 0.2026 pF, and 1.5 pF, respectively. One open stub connected to a tee-junction or two open stubs combined by a cross-junction are required to realise C2 if the conventional design technique is adopted. However, it can be realised by simple microstrip line which has more broad width than 50 Ω line impedance as shown in Fig. 4*b*. The width is fixed to 3.5 mm, which corresponds to the width of the 30 Ω microstrip line as shown in Fig. 1. Length '*G*' has been chosen as 5 mm after calculation of capacitance using the equation for the parallel plate capacitor. Because of the lower impedance of the microstrip line, the more capacitive equivalently, open stubs and junction elements are not required in realising the LPF by increasing the width of microstrip line in 'DGS section'. The increased line width of the LPF guarantees the capability of very high power handling.

The area of total DGS section is 149.5 mm^2, while that of a conventional LPF that we have designed as a reference, but is not shown here, using the step impedance technique for similar frequency responses is 305.1 mm^2. The size of the proposed LPF is only 49% of the conventional design. Although there are two 'step' discontinuities, they can be softened by adding smooth taper or triangle elements to the step sections.

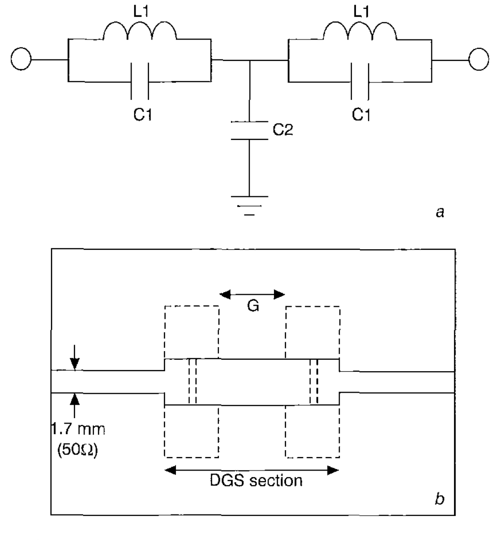

Fig. 4 *Schematic diagram of designed LPF, and the proposed LPF with two DGS patterns and compensated line width*

a Schematic diagram
b Proposed LPF

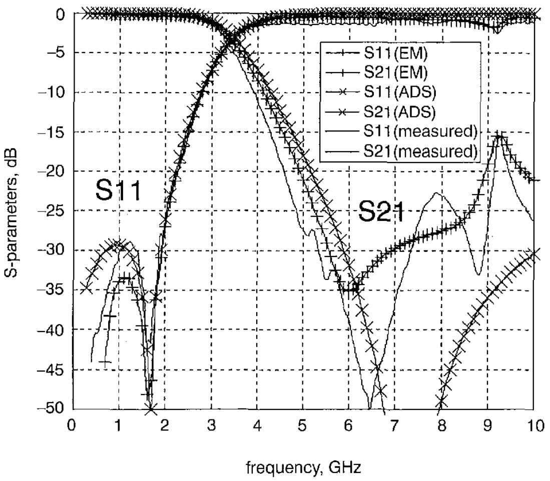

Fig. 5 *Measured performances of proposed LPF*

Measured results: Fig. 5 shows the predicted and measured performances of the LPF. Although minor discrepancy is observed due to the weak interaction between DGS patterns, which are not contained in the schematic diagram in Fig. 4*a*, a good agreement has been achieved.

Conclusion: A new LPF using only two DGS patterns and compensated microstrip line is proposed. No open stubs, high impedances lines, and tee- or cross-junction are required. This makes the proposed LPF suitable for high power application. Additionally, the required area for the LPF is only half that of the conventional LPF owing to the large equivalent elements that originate from the DGS pattern.

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Linearity of low microwave noise AlGaN/GaN HEMTs

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The linearity of low microwave noise AlGaN/GaN HEMTs was evaluated with two-tone excitation measurements at optimum low noise biases. A 0.15 × 100 μm^2 device yields an output third-order intercept point (OIP3) of 23 dBm at V_{ds} = 3 V, and V_{gs} = −5V, where a noise figure (NF) of 1.0 and 1.75 dB was obtained at 10 and 20 GHz, respectively. The C/IM3, linearity figure-of-merit under the large RF signals, saturates near −28 dBc as V_{ds} becomes greater than the knee voltage. Both applied bias and gate periphery dependence of the linearity were evaluated. Realisation of highly linear low-noise GaN HEMTs is feasible.

Introduction: Recently, there has been growing interest in implementation of GaN HEMT low-noise amplifiers (LNA), which enable a higher degree of survivability under the strong RF illumination [1–2]. Many microwave receiver applications require LNAs with high dynamic range, i.e. excellent linearity, in which the LNAs can handle strong input signals without generating excessive harmonic distortion. The linearity is often measured by a two-tone intermodulation measurement, where the linearity figure-of-merit is, in general, determined by third-order (IP3), and second-order (IP2) intercept points, or the ratio (C/IM3) of carrier power (C) over third-harmonic product (IM3). The linearity of FETs tends to increase with device size or high DC power. Conversely, the LNAs often require low DC power dissipation. Although the linearity evaluations of GaN HEMTs for transmitter applications have been recently reported [3–4], the characterisation of both noise figure and linearity on low-noise GaN HEMTs has been very limited to date.

In this Letter, we report both linearity and noise figure (NF) of low-noise AlGaN/GaN HEMTs at optimum low-noise biases. A 0.15 × 100 μm^2 device yields output IP3 (OIP3) of 23 dBm at V_{ds} = 3 V and V_{gs} = −5 V when a 3:1 slope is extrapolated, and NF of 1 dB was measured at 10 GHz with DC power dissipation of ~120 mW. The measured C/IM3 saturates near −28 dBc as $V_{ds} \geq 5$ V, close to the values observed at transmitter biases. Almost linear scaling of OIP3 was observed up to 0.3 mm gate periphery.