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BRIEF PAPER

Design of Wideband Coupled Line DC Block with Compact Size

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SUMMARY This letter proposes a wideband compact DC block design technique. This DC block has a wide pass-band and wide stop-band and transforms termination impedances. It comprises a pair of coupled lines on a defected ground structure (DGS) with capacitor loading. A periodic DGS pattern increases coupling, and, consequently, a wideband DC block design is allowed with a microstrip process on a high dielectric low height substrate. A DC block with equal termination impedances of 50 Ω and another that transforms 50 into 30 Ω are fabricated. The measured fractional bandwidths are 48% and 47%. The size of the DC block is $16.8 \times 15\,\text{mm}^2$ ($0.057\lambda_0 \times 0.051\lambda_0$).

key words: *Wideband DC block, Coupling enhancement, DGS, slow wave structure, Capacitance loading*

1. Introduction

With ever-increasing wireless communication services, a compact size wideband DC block has become a more important component. At the same time, a DC block with an impedance transforming characteristic is required to eliminate an additional matching network for noise matching of an LNA or power matching of a PA [1], [2]. In addition, a wide stop-band characteristic is desirable for the receiver design [3]. In previous works, a cymbal type DC block was proposed for a wideband DC block [4]. However, [4] this does not provide an exact DC block design equation and a design method for different termination impedances. A distributed coupled DC block design equations for equal and different termination impedance are provided [5], but the length of the coupled line is fixed at a quarter-wavelength; therefore, this DC block has a long length [2], [5]. Spurious frequency also occurs at the third-harmonic frequency. These problems were overcome in [6]; however, the structure in [6] requires grounded coupled lines or series inductors. The grounded coupled lines cannot be used for DC blocks. The series inductor is an unattractive component because it generally has a poor quality factor and its maximum value is limited in fabrication [7]. Moreover, the bandwidth is limited because the maximum mutual coupling coefficient is restricted by a given substrate and microstrip process [5]. It becomes more problematic when using a high dielectric, low height substrate for compact DC block design.

In the present study, a defected ground structure (DGS) is exploited to overcome these problems. A periodic DGS not only makes a slow wave but also enhances coupling between a pair of coupled lines. A slow wave allows a compact DC block design, and an enhanced coupling coupled line allows a wideband DC block design on a high dielectric low height substrate. Capacitance loaded transmission lines and DGS slots are also exploited to attain a more compact DC block and to increase stop-band.

Transmission lines on a periodic DGS resonate with loaded capacitors on a center frequency. Therefore, they are modeled by two resonators with J-inverters for a center frequency. Therefore, if we assume the notch slots have little effect on pass-band operation, then the general second order filter design equation can be directly applied, and this filter design equation allows us to know all the design parameters when the termination impedances, bandwidth, and the filter type are determined. The proposed DC block is shown in Fig. 1. Due to a DGS, a coupling (J2) between resonators is enhanced compared with conventional structure. The equivalent circuit is shown in Fig. 2.

2. Analysis and Design

For a wideband DC block design, a high coupling structure is needed. In [8], a large square aperture structure is pro-

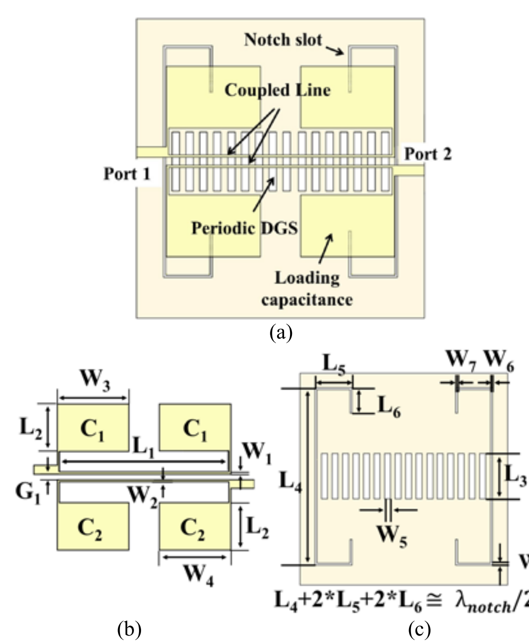

Fig. 1 The proposed DC block. (a) Overall-view, (b) top-view, and (c) bottom-view.

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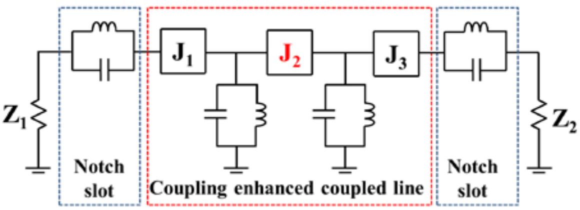

Fig. 2 The equivalent circuit of the proposed DC block.

posed to enhance the coupling. However, this increases the circuit size due to its high wave propagation velocity. In this study, we focus on a periodic square DGS pattern to enhance the coupling while decreasing wave propagation velocity for a compact DC block.

DGS patterns are normally used to achieve a filtering effect or slow wave effect. However, in this study, we focus on a periodic DGS pattern to increase the coupling between two coupled lines. This DGS pattern makes the larger the difference between the even- and odd-mode impedance. Consequently, it increases coupling between two coupled lines. A square DGS pattern is considered a suitable pattern; due to its layout shape that allows several slots to be easily inserted in restricted area, and the width and length of the slots to be easily adjusted. Therefore, slow wave factor and coupling magnitude are controlled with ease.

For more compact size DC block design, a capacitance loading technique is adopted. It helps to decrease the transmission line length and expand the stop-band [9]. However, stop-band expansion is limited due to the loading capacitor value being restricted by its size. Therefore, the notch slots are also used for stop-band expansion. These slots act like a notch filter. Folded type slots are used to design a compact size DC block.

For a proposed DC block implementation, first, we investigate the characteristic impedance Z_0 and the electric length θ of the transmission line on a periodic DGS slots. It can be carried out by an EM simulation.

Second, we obtain loading capacitor values. The capacitance of the patch, C_1, is determined by

$$C_1 = \frac{1}{2\pi f_0 Z_0 \tan(\frac{\theta}{2})} \quad (1)$$

where f_0 is the center frequency. C_2 is also determined using the same equation.

Third, we decide the initial parameter. The following design equations can be used for determining the initial parameter values.

$$Q_1 = \frac{g_0 g_1}{FBW}, \quad Q_2 = \frac{g_2 g_3}{FBW} \quad (2)$$

$$M_{12} = \frac{FBW}{\sqrt{g_1 g_2}} \quad (3)$$

where g_0, g_1, g_2, and g_3 are the low-pass prototype parameters, given for a normalized low-pass cutoff frequency $\Omega_c = 1$, Q_1, and Q_2 are the external quality factors of the resonators, and M_{12} is the coupling coefficients between the resonators. DC blocks have the same operation if these initial parameters are same. This implies that impedance transform can be achieved by meeting these initial parameters.

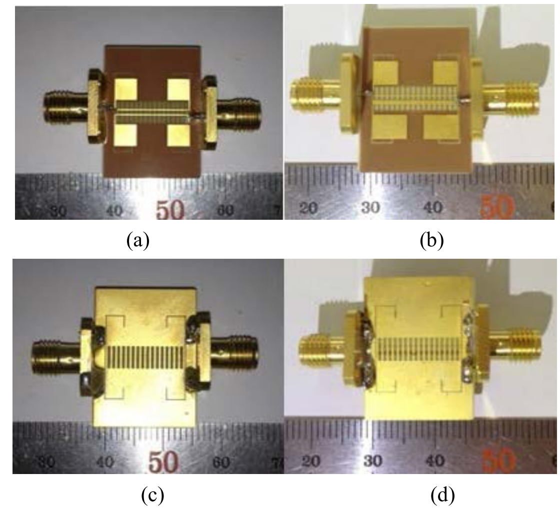

Fig. 3 The fabricated DC blocks. (a), (c) : 50 and 50 Ω terminated DC block top and bottom view. (b), (d) : 50 and 30 Ω terminated DC block top and bottom view.

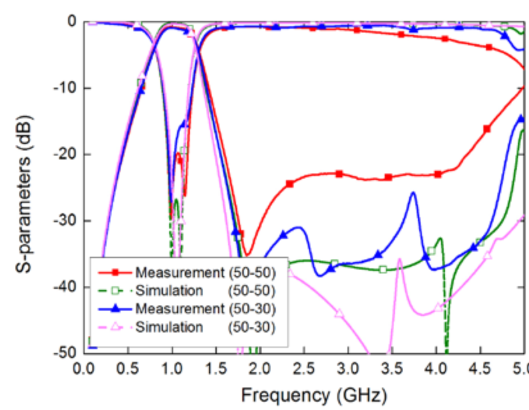

Fig. 4 The simulation and measurement results: 50 and 50 Ω terminated DC block and 50 and 30 Ω terminated DC block.

Due to the external qualify factor of each resonator being proportional to the termination impedance, when the termination impedance is lower, the transmission line width of the resonator with lower termination impedance must be extended for increasing susceptance slope. In the opposite case, the line width must be shrunk.

Finally, we insert DGS notch slots, which are shown in Fig. 1. These slots increase the stop-band. These notch slots are modeled by a series connected parallel resonators. A bent-slot is used to reduce the area of the circuit. The total length of the notch slots, $L_4 + 2 * L_5 + 2 * L_6$, is equal to $\lambda_{notch}/2$, where λ_{notch} is the wavelength at the notch frequency. The simulated result (50–50 Ω terminated DC block with/without slots) shows that the stop-band ($|S_{21}|$ 20 dB attenuation reference) is extended to around 850 MHz, which corresponds to 85% of the center frequency.

The proposed DC block has a large ratio of notch-band frequency to pass-band frequency due to its use of the peri-

Table 1 Design parameters.

Unit: mm	50–50 Ω terminated	50–30 Ω terminated
W_1	0.15	0.15
W_2	0.15	0.6
L_1	12.8	12.8
G_1	0.8	0.8
W_3	3.75	3.75
W_4	3.75	5.15
L_2	4	4
W_5	0.52	0.52
L_3	4	4
$W_6 = W_7 = W_8$	0.15	0.15
L_4	15	15
L_5	3.15	3.15
L_6	2.15	2.15

Table 2 Comparitve summary about the bandwidth, size, impedance transformation, filter type and gap (G_1) of DC blocks.

	FBW (%)	Size ($\lambda_0 \times \lambda_0$)*	Impedance transformation	Filter type	gap (mm)
This work	47	$0.057\lambda_0 \times 0.051\lambda_0$	○	Butterworth	0.8
Ref. [4]	10	$0.387\lambda_0 \times 0.134\lambda_0$	×	Not Specified	0.37
Ref. [5]	50**	$0.008\lambda_0 \times 0.17\lambda_0$	○	Butterworth	0.25
Ref. [6]	9.2	$0.237\lambda_0 \times 0.169\lambda_0$	Not Specified	Chebyshev	Not Specified

* λ_0 is the wavelength in the free space at the center frequency.
** FBW is estimated by figure.

odic DGS pattern and capacitance loading. Therefore, these notch slots rarely affect pass-band operation. However, in case these notch slots significantly affect pass-band performance, a physical parameter modification and optimization step is required to meet the bandwidth.

3. Implementation and Measurement

The feasibility of the proposed wideband DC block is verified through measurements of a design consisting of one DC block with 50 Ω to 50 Ω termination impedances and another one transforming 50 into 30 Ω at the center frequency of 1 GHz. They are fabricated on a high dielectric, low height, highly lossy substrate (FR-4 with $\varepsilon_r = 4.6$, $H = 0.2$ mm and $\tan\delta = 0.25$). The design parameters are shown in Table 1. The fabricated circuits are shown in Fig. 3, and the simulated results are compared with the measured ones in Fig. 4. The simulation and measurement results are well matched in both cases. The measured $|S_{21}|$s are −0.79 dB and −0.91 dB around the center frequency, and the 3-dB bandwidths are 0.80–1.29 GHz and 0.806–1.286 GHz (48% and 47%), respectively. The proposed DC block accomplishes wideband performance and the corresponding coupling coefficient on a high dielectric, low height substrate and the gap (G_1) of two coupled lines is wide (0.8 mm). It implies that the proposed structure has successfully solved the coupling strength problem. The insertion loss looks slightly high, since an FR-4 substrate is a highly lossy material. The size of the proposed DC blocks are 16.8×15 mm^2 ($0.057\lambda_0 \times 0.051\lambda_0$), where λ_0 is the wavelength in the free space at the center frequency. Table 2 gives a summary about the bandwidth, size, impedance transformation, filter type and gap of DC blocks.

4. Conclusion

In this letter, we have introduced a new DC block structure. It has wide pass-band, wide stop-band, and an impedance transforming property with compact size. This structure successfully overcomes the coupling strength problem by exploiting a periodic DGS. One DC block with equal termination impedance and another with unequal termination impedance were fabricated and measured. They have 48% and 47% fractional bandwidth, respectively. The measurement results tally with the simulation results. The proposed DC block is appropriate for compact microwave components and monolithic microwave integrated circuits (MMICs).

Acknowledgments

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References

[1] H.-R. Ahn and B. Kim, "Toward integrated circuit size reduction," IEEE Microw. Mag., vol.9, no.1, pp.65–75, Feb. 2008.
[2] M. Abbasi, H. Zirath, and I. Angelov, "Q-, V-, and W-band power amplifiers utilizing coupled lines for impedance matching," Proc. IEEE MTT-S Int. Microwave Symp. Dig., pp. 863–866, June 2008.
[3] A. A. Abidi, "The path to the software-defined radio receiver," IEEE J. Solid-State Circuits, vol.42, no.5, pp.954–966, May 2007.
[4] B. Strassner and K. Chang, "New wide-band DC-block cymbal bandpass filter," IEEE Trans. Microw. Theory Tech., vol.50, no.5, pp.1431–1432, May 2002.
[5] H.-R. Ahn and T. Itoh, "Impedance-transforming symmetric and asymmetric DC blocks," IEEE Trans. Microw. Theory Tech., vol.58, no.9, pp.2463–2474, Sept. 2010.
[6] S. Lee and Y. Lee, "Generalized miniaturization method for coupled-line bandpass filters by reactive loading," IEEE Trans. Microw. Theory Tech., vol.58, no.9, pp.2383–2391, Sept. 2010.
[7] J. S. Hong and M. J. Lancaster, Microstrip Filters for RF/Microwave Applications, Wiley, 2001.
[8] L. Zhu, H. Bu, and K. Wu, "Aperture compensation technique for innovative design of ultra-broadband microstrip bandpass filter," IEEE MTT-S Int. Microwave Symp. Dig., pp.315–318, June 2000.
[9] J.-S. Hong and M. J. Lancaster, "Theory and experiment of novel microstrip slow-wave open-loop resonator filters," IEEE Trans. Microw. Theory Tech., vol.45, no.12, pp.2358–2365, Dec. 1997.