A Two-Stage *S*-/*X*-Band CMOS Power Amplifier for High-Resolution Radar Transceivers

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***Abstract*— This paper presents a reconfigurable *S*-/*X*-band power amplifier (PA) integrated into a 0.18-μm RF CMOS process. A switchable transformer for output matching is operated by tuning its primary winding and a shunt capacitor under a 50-Ω load with passive efficiency of more than 63%/67% for the *S*-/*X*-band. Series resonant circuits with bond wires are employed at common-mode nodes, greatly improving the *X*-band performance of the PA. Despite the use of interstage matching without any tunable elements, the PA presents a power gain of more than 19.5 dB at both 3 and 8 GHz. The PA provides saturated output power of 24.8/21.5 (21.5) dBm with a power-added efficiency of 32.8%/11.1% (10.7%) at 3/8 (9) GHz. The 1-dB bandwidth is 0.6/2 GHz (2.8–3.4/7.5–9.5 GHz) for the *S*-/*X*-band. This amplifier demonstrates suitable performance for dual-band high-resolution radar transceivers.**

***Index Terms*— CMOS, dual band, power amplifier (PA), radar transceiver, reconfigurable, switchable transformer.**

I. Introduction

MODERN radar systems often require multiband operations due to different characteristics of environments and targets. For example, *S*-band signals are resistant to severe weather and atmospheric attenuation. On the other hand, frequencies on the *X*-band are often used for highly resolved target imaging. Although CMOS technology has become an attractive solution for low-cost high-integration systems, achieving dual-band functionality in a fully integrated CMOS power amplifier (PA) has been challenging. Most current CMOS PAs do not meet the requirements of radar systems using the aforementioned frequency bands and some of them are realized by multiple PAs that are optimized at each target frequency [1].

Several approaches have been developed to implement broadband or multiband features in a single PA. For example, high-order passive networks, stacked stepped-impedance transformers, and switchable transformers have been introduced [2]–[5]. However, when employing high-order networks for the *S*-/*X*-band, the passive efficiency decreases rapidly in the lower/upper band with excessive area for multiple inductors. Moreover, optimal load matching on the *S*-/*X*-band cannot be realized by transformers alone in CMOS due to the limited coupling factor. Switchable transformers for multiband capabilities have been suggested, but using only variable capacitors, as in [5], cannot achieve optimal loads on multiple operating frequencies which are set broadly.

In this paper, the designed PA is intended for *S*-/*X*-band FMCW radar systems which detect a target through obstacles in a short range. Because the range resolution is inversely proportional to the chirp bandwidth, radar requires a 3-dB bandwidth ($BW_{3\text{-dB}}$) wider than 1.2 GHz at each band to detect small targets (13 cm). In addition to the reconfigurable output matching network (OMN) for a single-stage PA proposed in [6], this letter explains the design of a multistage PA and shows the effectiveness of a simple resonant technique to alleviate the asymmetry of differential-load effects on the *X*-band.

II. Dual-Band CMOS PA Architecture

A. Design of the Reconfigurable Dual-Band Transformer

The optimal load impedances of a differential cascode are calculated by load-pull simulations at 3/8.5 GHz. The OMN has to be configured differently for each frequency, and a smaller value of the shunt inductance in the OMN is required to resonate with the device output capacitance as the frequency increases. As illustrated in Fig. 1, an equivalent circuit of a high-Q transformer and additional capacitors (C_1 and C_2) are employed for the OMN. Assuming that the coupling factor is 0.7 and that the quality factor is 10, transformed impedance was simulated for two cases. First, the load impedance (Z_{Load}) was calculated by varying C_1 (0.1–2 pF) and C_2 (0.8–2 pF), maintaining L_1 (0.36 nH), and optimizing L_2 (0.73 nH) on the *X*-band. Second, to achieve Z_{opt} for the *S*-band, the trajectories of Z_{Load} were drawn by varying L_1 (0.2–0.75 nH) and C_2 (0.8–2 pF) and keeping C_1 (1.43 pF) fixed on the *S*-band. As L_1 increases the real/imaginary parts of Z_{Load}, and C_2 precisely controls Z_{Load} to Z_{opt}, higher L_1 (0.58 nH)/C_2 (1.56 pF) and lower L_1 (0.36 nH)/C_2 (1.24 pF) values are required for the *S*- and *X*-bands, respectively, with fixed values of C_1 (1.43 pF) and L_2 (0.73 nH).

The proposed reconfigurable OMN is shown in Fig. 2(a); L_1 increases for the *S*-band due to the inner turn winding and C_2 decreases for the *X*-band due to the OFF-capacitance (C_{OFF}) of S2. To ensure proper operations, S1/S2 is turned OFF/ON for the *S*-band, while S1/S2 is turned ON/OFF for the *X*-band. To maintain high passive efficiency on the *X*-band, a gap of 40 μm exists between the conventional and inner primaries. With a C_{OFF} value of 1.69 pF and R_{on} equal to 0.9 Ω for S1, the peak passive efficiencies of the proposed transformer show 64.5%/68.5% on the *S*-/*X*-band, as shown in Fig. 2(b). Moreover, with a C_{OFF} value of 0.35 pF for S2, the designed load impedances at 3/8.5 GHz are

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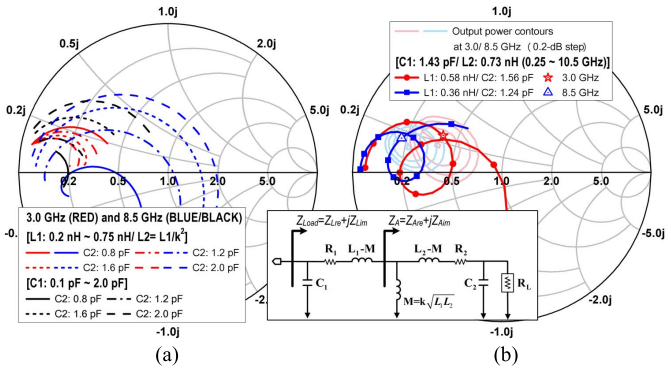
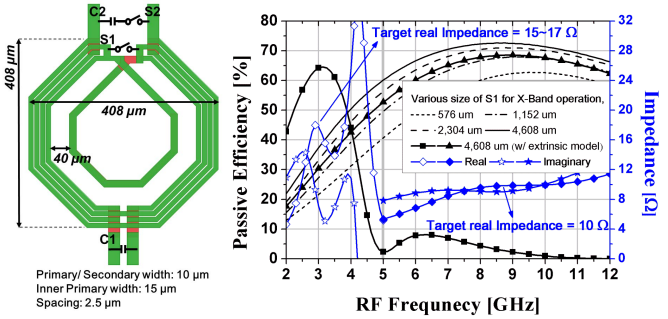


(a) (b)

Fig. 1. (a) Normalized Z_{Load} with variations of L_1, L_2, C_1, and C_2 at 3 and 8.5 GHz. (b) Normalized Z_{Load} with optimized L_1, L_2, C_1, and C_2 according to the frequency (0.25–10.5 GHz).



(a) (b)

Fig. 2. (a) Physical layout of the OMN. (b) Passive efficiencies with various sizes of S1 and complex load impedances for *S*-/*X*-band operation.

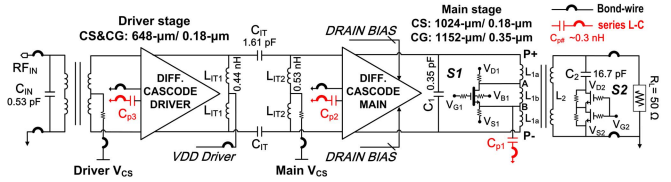


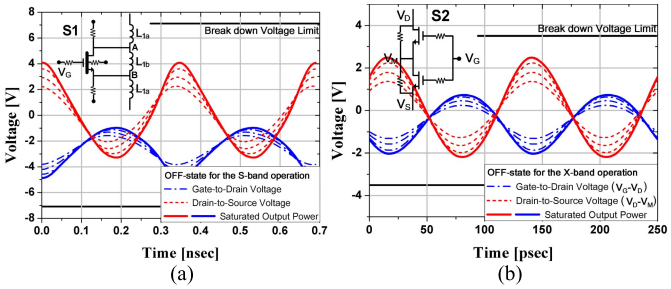
Fig. 3. Overall schematic of the designed dual-band CMOS PA.

$15.5 + j15.8\ \Omega / 11.02 + j9.54\ \Omega$, respectively, which are well located in the load-pull contours.

B. Two-Stage S-/X-Band PA With Resonant Circuits

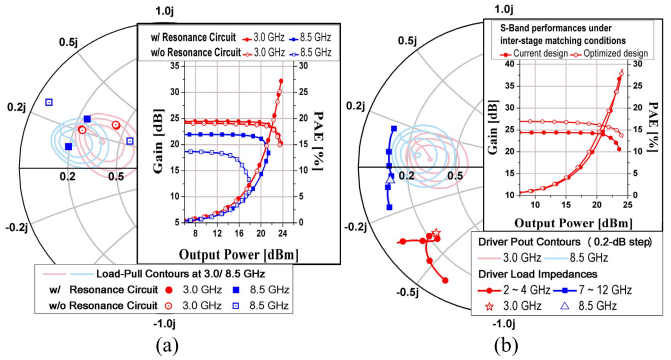
A detailed circuit schematic of the dual-band CMOS PA is presented in Fig. 3. S1 (4.608 mm/0.35 μm) and S2 (1.152 mm/0.18 μm) are implemented by a thick-gate-oxide transistor and two stacked transistors, respectively, which have good reliability up to a peak-to-peak voltage of 7.2 V. As illustrated in Fig. 4, the maximum drain-to-source/gate-to-drain voltage differences of S1 and a single transistor in S2 for the OFF-state are close to 4/5 and 2.5/2 V at the saturated output power, respectively.

The practical layout of the OMN cannot be perfectly balanced due to different inner-connection metals, and this causes severe asymmetry in a differential load during the *X*-band operation. To alleviate these effects, capacitors (C_{p2} and C_{p3}) with series bond wires, resonating at 8.5 GHz, are employed at the source nodes of the differential driver/main amplifiers. A smaller capacitor (C_{p1}) with the bond wire is also utilized at the center tap of the conventional primary. These resonant circuits are forcibly shown as the ac-ground on the *X*-band, and they relieve the asymmetric effects. As shown in Fig. 5(a), for the *X*-band operation, a differential load moves



(a) (b)

Fig. 4. Simulated voltage difference waveforms of (a) S1 and (b) S2 in the OFF-state.



(a) (b)

Fig. 5. (a) Normalized Z_{Load} of the OMN with and without a resonant circuit. (b) Normalized Z_{Load} of the driver amplifier with the designed interstage MN.

into the load-pull contours, and the 1-dB compression output power (P1dB) is improved by more than 4 dB. Moreover, for the *S*-band operation, the resonant circuits and multibond wires at the differential source nodes provide lower impedance, thus improving the P1dB performance (~0.4 dB).

Considering interstage matching in a two-stage PA, higher shunt inductance (L_{IT2}) is required for the *S*-band to cancel out the gate capacitance in the main amplifier. To control L_{IT2} using paralleled switches, the interstage MN undergoes an additional loss/excessive area and demands negative voltages. As shown in Fig. 5(b), although the designed interstage mismatch appears to be somewhat severe for the *S*-band operation, the peak power gain and power-added efficiency (PAE) of the designed PA are in fact reduced by 2.57 dB and 1.69%, respectively. This small degradation in the *S*-band is caused by the relatively low-*Q* interstage matching, though it still presents a power gain of nearly 25 dB. For the *X*-band operation, an input balun optimized for the *X*-band compensates for the power gain which was degraded due to the slight interstage mismatch.

The total gate widths of the common source/gate for the main stage are 1024/1152 μm with a gate length of 0.18/0.35 μm, under a supply of 3.6 V. For the driver stage, the transistor (648/0.18 μm) is chosen for a differential pair of cascode topologies with a supply of 1.8 V.

III. Measurement Results

The proposed two-stage *S*-/*X*-band PA is fully implemented in a 0.18-μm 1P6M RF CMOS process that provides a 4.6-μm-thick aluminum layer as the top metal layer. Fig. 6 shows a photograph of the fabricated CMOS PA IC, which is mounted on a Duroid 5880 printed circuit board for the measurement. When presenting the highest P1dB performance for the *S*-/*X*-band, the driver and main stage consume 10/105 and 226/260 mA of dc current, respectively.

TABLE I

COMPARISON OF STATE-OF-THE-ART CMOS MULTIBAND PAS

Ref.	Freq. [GHz]	OMN Configuration	OMN Efficiency [%]	P_{SAT} [dBm]	PAE [%] (DE)	Tech. [nm]	VDD [V]	Chip Size/ PA Core [mm^2]	OMN Size [mm^2]	Fully Integration
[2]	2.0/6.0	1 *TF+3 inductors (Single IN-Single OUT)	N.A.	22.4/20.1	28.4/19	65	3.3	0.89/0.68	0.19	YES
[3]	5.2/13.0	1 TF+1 inductor (Single IN-Single OUT)	[1]30.0/45.0 58.6 @8.0 GHz	[2]20.0/23.0	[2]9.0/12.0 (N.A.)	90	2.8	0.697/N.A.	N.A.	YES
[4]	3.5/9.5	1 TF (Single IN-Single OUT)	[3]35.0/70.0 77.0 @5.5 GHz	[4]19.5/19.0	[4]20.0/19.0 (24.0/20.0)	40	1.2	1.4/N.A.	N.A.	YES
[7]	2.6/4.5	1 TF (#Diff. IN-Single OUT)	78.5/62.0	28.1/26.0	35.0/21.2 (40.7/27.0)	65	3.0	2.25/0.96	0.165	YES
[8]	2.0/2.9	2 TFs (Single IN-Single OUT)	N.A.	29.8/29.8	[5]23.0/25.6	180	3.3	2.4/N.A.	0.4	NO (series L-C w/ bond wire)
This work	3.0/9.0	1 TF+2 switches (Single IN-Single OUT)	[6]64.2/68.5	24.8/21.5	32.8/10.7 (33.2/11.6)	180	3.6	1.06/0.79	0.276	NO (series L-C w/ bond wire)

[1]Values taken from Fig. 10 in [3]. [2]Values taken from Fig. 14 in [3]. [3]Values taken from Fig. 3 (c) in [4]. [4]Values taken from Fig. 5 in [4]. [5]Values taken from Fig. 11 (b) in [8]. [6]Includes the parasitic of S1. *TF: Transformer. #Diff.: Differential.

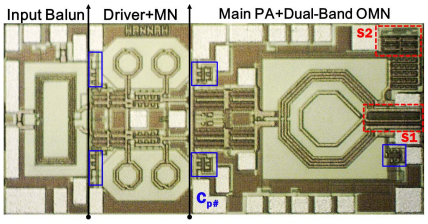


Fig. 6. Chip microphotograph of the CMOS PA (size = 1.67 mm 0.64 mm).

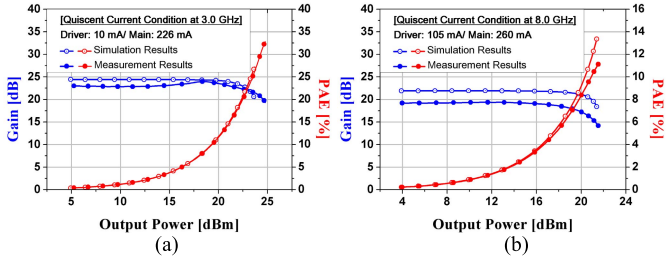


Fig. 7. Simulated/measured gain and PAE as a function of the output power with CW sources at (a) 3 and (b) 8 GHz.

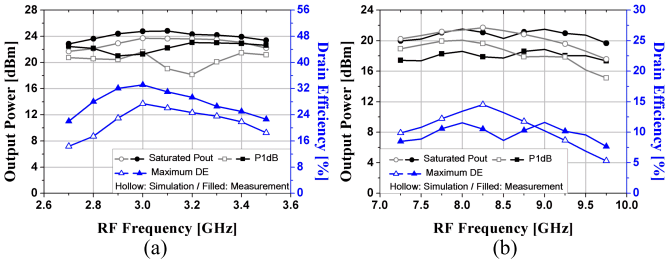


Fig. 8. Simulated/measured P_{SAT} and drain efficiency versus the frequencies for (a) *S*- and (b) *X*-band operations.

The $BW_{3\text{-dB}}$ according to S21 is 2.8–4/7.7–9.4 GHz during *S*-/*X*-band operation.

With continuous-wave (CW) sources at 3/8 GHz, Fig. 7 shows that the saturated output power (P_{SAT}) is 24.8/21.5 dBm with a peak PAE of 32.8%/11.1% and a corresponding maximum power gain of 24/19.5 dB. The PA also generates a P_{SAT} value of 21.5 dBm with a PAE of 10.7% at 9 GHz. The 1-dB bandwidth ($BW_{1\text{-dB}}$) depending on P_{SAT} is 2.8–3.4/7.5–9.5 GHz (FBW: 19.4%/23.5%), presenting more than 23.7/20.2 dBm for the *S*-/*X*-band, respectively, as shown in Fig. 8. The discrepancies between the simulated and measured data in Figs. 7 and 8 are mainly due to the imperfect large signal/electromagnetic modeling of the CMOS.

Table I compares the overall characteristics of the designed PA and other fully integrated CMOS PAs capable of multiband operation. The OMNs in most listed amplifiers cannot provide high passive efficiencies (above 64%) or optimized loads on the *S*-/*X*-band.

IV. CONCLUSION

A reconfigurable dual-band PA integrated into a CMOS is presented in this paper. This PA consists of a differential driver/main stage with an input/output matching network, operating on the *S*-/*X*-band. An integrated switchable transformer for the OMN provides optimal load impedances and high efficiencies on the *S*-/*X*-band. A series resonant *L*–*C* structure with a bond wire for the *X*-band is introduced into the PA and compensates for the degradation caused by the asymmetric differential load. A PA with tunable elements only in the OMN generates a maximum power gain of 24/19.4 (16.3) dB and a P_{SAT} of 24.8/21.5 (21.5) dBm with a PAE of 32.8%/11.1% (10.7%) at 3/8 (9) GHz, respectively. With a $BW_{1\text{-dB}}$ of 2.8–3.4/7.5–9.5 GHz, the proposed PA is conducive to further integration with additional transceiver circuits to form a dual-band high-resolution radar system on a chip.

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