High-Efficiency Harmonic Loaded Oscillator with Low Bias Using a Nonlinear Design Approach

Moon-Que Lee, *Member, IEEE*, Seung-June Yi, Sangwook Nam, *Member, IEEE*, Youngwoo Kwon, *Member, IEEE*, and Kyung-Whan Yeom, *Member, IEEE*

***Abstract*—We present a design method for an optimized high-efficiency harmonic loaded oscillator. The proposed approach predicts the performance of oscillators including output power, dc–RF conversion efficiency, and dc-bias current shift during start-up transition. In this method, the performance of the oscillator can be optimized based on the performance analysis of the active device under the assumed operation conditions. The effects of fundamental and harmonic loading on output power and efficiency are investigated by the proposed approach. Two kinds of stability conditions are addressed for an oscillator initially biased at a low gate voltage. Using the proposed approach, we design an oscillator that has a high efficiency of 61% at 1.86 GHz with a very low bias voltage of 2.0 V.**

***Index Terms*—Harmonic loaded oscillator, harmonic loading, high-efficiency oscillator, load line, microwave oscillator, oscillator stability, stability.**

I. Introduction

An oscillator can be viewed as an active device with an external feedback network. The feedback network elements are usually determined in order for the active device to deliver maximum output power to the load. To maximize the output power, it is required to correctly characterize the active device by small- or large-signal linear parameters or nonlinear device models. A number of oscillator design methods have been reported that use large-signal S- or Y-parameters obtained from measurement [1]–[4] or modified small-signal S-parameters [3], [5]. These quasi-nonlinear techniques are simple, but their accuracies are valid only when the harmonic components are negligible or small enough compared with the fundamental frequency component. Hence, these approaches fail to predict the performance correctly for cases in which oscillators operate in a saturated region. Other oscillator design approaches have been studied to include the nonlinearities more precisely with nonlinear device models [6]–[8], but they are analysis-based approaches rather than synthesis-based ones. Although Berini [9] investigated experimentally the harmonic effects on output power of an oscillator, no paper has yet been reported that explicitly deals with harmonic effects. In this paper, we present a nonlinear design method for a harmonic loaded oscillator and clearly show the effects of fundamental load and harmonic load on the performance of an oscillator.

The contents of this paper are as follows. In Section II, we present a systematic nonlinear oscillator design approach which can precisely deal with nonlinear phenomena, including output power, efficiency and harmonic effects. In this approach, the embedding network elements are synthesized through the analysis of the RF operating point of the active device. In Section III, we discuss the load lines for maximum power and for maximum dc–RF conversion efficiency. In Section IV, we investigate start-up and build-up criteria for oscillators. The start-up criterion is a microwave representation of the Nyquist stability criterion using the S-parameters. The build-up condition tells us whether the noise signal satisfying the small-signal oscillation condition grows up to the steady state. To verify the validity of the proposed design method, a harmonic loaded oscillator is designed and tested in Section V.

II. Nonlinear Design Method

A. Substitution Theory

When an active device is given, it is generally difficult to assess whether a designed oscillator has the optimum performance in its output power or efficiency. This is because there are a lot of different types of oscillators and the tuning of the embedding circuits may change the oscillation frequency and output power simultaneously. Fig. 1 shows the scheme of the oscillation analysis in commercial harmonic-balance computer-aided design (CAD).[1] It uses OSCTEST for the analysis of a general oscillator. OSCTEST is used to inject a signal to the oscillator and to check whether or not the oscillation condition is met. The oscillation occurs when the loop gain is unity. The active device operates at the RF-drive level of the injected power of OSCTEST when the oscillation condition is satisfied. Small variations in the circuit parameters in Fig. 1 change the oscillation frequency and output power at the same time. Hence, it is not easy to design an embedding network for the optimum performance of an oscillator using the method described above. In order

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[1] *HP-EEsof Libra Manual*, Hewlett-Packard Company, Santa Rosa, CA, 1993.

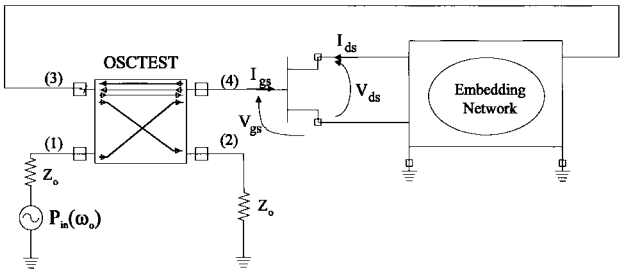


Fig. 1. Oscillator analysis using OSCTEST in conventional CAD (HP-Libra).

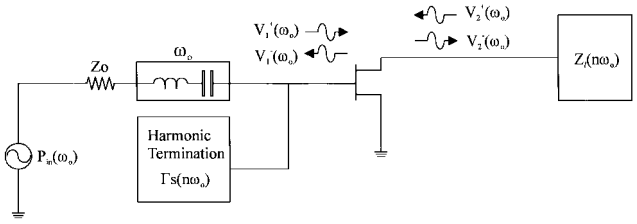


Fig. 2. Scheme of the impedance substitution for the embedding network.

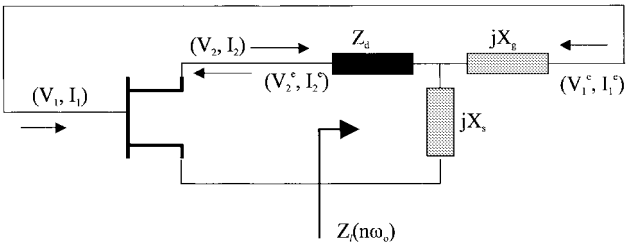


Fig. 3. An oscillator topology with T-shaped embedding elements.

to overcome this difficulty, we notice that the output power of an oscillator is related to the RF drive level of OSCTEST and the terminal voltages and currents $v_{\rm gs}$, $v_{\rm ds}$, $i_{\rm gs}$ and $i_{\rm ds}$, shown in Fig. 1. Since an oscillator is viewed as an active device with an external feedback network, it is a timesaving approach to analyze an oscillator by separating it into an active device and an external feedback network. Also, the external feedback network can be substituted with the terminal impedance of the active device to avoid the nuisance that many different embedding networks may yield the same terminal voltages and currents to the active device. Consequently, the design problem is now reduced to the determination of the RF drive level ($|V_{1,RF}^{+}(\omega_o)|$) corresponding to the injection signal of OSCTEST and load termination [$Z_l(n\omega_o)$] at the desired frequency. The detailed procedure for the determination of the RF-drive level and the terminal impedance will be explained in Section III. Once the terminal voltages and currents are determined, the embedding network is directly synthesized using the simple circuit theory. In the substitution for the embedding network described above, the following two facts are assumed: 1) similar to the simulation using OSCTEST, all the harmonics are generated by the fundamental incident wave V_1^+ and 2) since $Z_l(n\omega_o)$ is the impedance looking into the feedback loop at the drain–source terminal, this may be assumed passive.

In the above approach, the net power delivered to the load and the dc–RF conversion efficiency are defined by

$$P_{\rm osc}(\omega_o) = \frac{1}{Z_o}\left[\left\{|V_1^-(\omega_o)|^2 - |V_1^+(\omega_o)|^2\right\} + \left\{|V_2^-(\omega_o)|^2 - |V_2^+(\omega_o)|^2\right\}\right] \quad (1)$$

$$\eta = \frac{P_o(\omega_o)}{|V_{\rm DS}I_{\rm DS}| + |V_{\rm GS}I_{\rm GS}|} \quad (2)$$

where Z_o is the normalization impedance of the S-parameters, and $V_{\rm DS}$, $I_{\rm DS}$, $V_{\rm GS}$ and $I_{\rm GS}$ are terminal dc voltages and currents applied to the active device.

B. Synthesis of the Embedding Network

The net power of (1) will be reproduced as the fundamental output power of the oscillator if the embedding feedback network of the oscillator is synthesized for the terminal voltages and currents to be the same as those of Fig. 2. Once the terminal voltages and currents are determined using the above approach, it is possible to obtain the values of all elements of the generalized six basic oscillator configurations: three shunt topologies and three series topologies. For the series feedback topology of Fig. 3, which has a load connected to the drain port, the embedding elements are uniquely determined by

$$Z_d = z_2 + j\beta_b\frac{\rm Re\{z_1\}}{\rm Im\{\beta_f\}} \quad (3)$$

$$jx_s = j\frac{\rm Re\{z_1\}}{\rm Im\{\beta_f\}} \quad (4)$$

$$jx_g = j\,{\rm Im}\{z_1\} = j{\rm Re}\{z_1\}\frac{\rm Re\{\beta_f\}}{\rm Im\{\beta_f\}} \quad (5)$$

where z_1, z_2, β_f, and β_b are defined in Appendix I.

III. Load-Line Analysis: Determination of Optimum RF Drive Level and Harmonic Load Line

A. Analytic Load Line for a High-Efficiency Oscillator with Low Drain Bias

As explained in the previous section, the design of an oscillator with high efficiency is directly related to the load line of an amplifier with high efficiency. In an amplifier design, the improvement of dc-to-RF efficiency is generally obtained by using highly driven class-B or class-F amplification terminated by proper harmonic terminations. In such a case, the waveform of the drain current becomes a pulsed shape, while the drain voltage is maintained sinusoidal with the harmonic voltages shorted. Further improvements in output power and efficiency are obtained when the drain voltage becomes a square wave, especially for a low drain bias [10]. As described above, the optimum load impedance has been studied for maximum drain efficiency. In this paper, only the fundamental and second harmonic impedances are taken into account in the implementation of the load impedance. The optimum loads

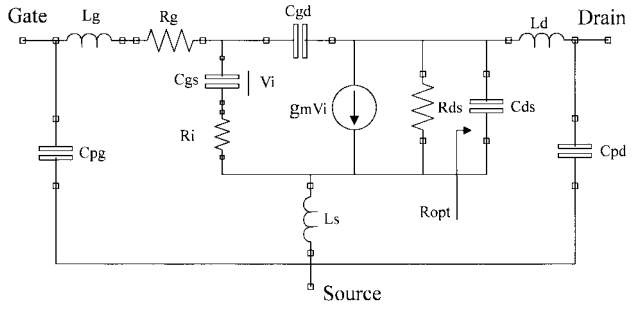


Fig. 4. An equivalent circuit of MESFET or HEMT. $R_{\rm opt}$ is the resistance looking into the load at the drain-current source.

are given as follows:

$$R_{\rm opt}(\omega_o) = \frac{8}{\pi}\frac{V_{\rm DS}-V_{\rm SAT}}{I_{\max}}$$
$$R_{\rm opt}(2n\omega_o) = 0$$
$$R_{\rm opt}\{(2n+1)\omega_o\} = \infty \tag{6}$$

where $V_{\rm SAT}$ is the drain saturation voltage, $I_{\max}$ is the maximum drain current and $n = 1, 2, 3, \cdots$.

Fig. 4 shows the equivalent circuit of MESFET or high electron-mobility transistor (HEMT) with parasitic elements. In the derivation of (6), the active device is assumed to be an ideal voltage-controlled current source without an internal resistance. However, a real transistor has an internal resistor $R_{\rm ds}$. Therefore, a portion of the generated output power may be dissipated in the internal resistor $R_{\rm ds}$. In order to eliminate the parasitic elements' effects, the terminal impedance for $R_{\rm opt}$ should be calculated. The terminal impedance compensating for the parasitic elements is given by

$$Z_{\rm opt}(n\omega_o) = \frac{1}{\dfrac{1}{\dfrac{1}{\dfrac{1}{R_{\rm opt}(n\omega_o)} - jn\omega C_{\rm ds}} - jn\omega(L_d+L_s)} - jn\omega C_{pd}} \tag{7}$$

where n is the order of harmonics.

Fig. 5 shows the results of the active device analysis (ADA) for HEMT (Fujitsu FHX35LG) with the harmonic load of (7) at $V_{\rm GS} = -0.5$ V and $V_{\rm DS} = 2$ V. The simulation is performed by HP-Libra with the EEHEMT3 model. From Fig. 5, we note that, for the oscillator initially biased near pinchoff, the dc drain current significantly increases as the RF-drive level increases. In proportion to the dc drain current, the output power and conversion efficiency also increase until the gate–source Schottky barrier is turned on. The maximum dc-to-RF conversion efficiency occurs at the point where the gate–source Schottky barrier begins to be turned on, while the maximum output power is observed at slightly above the gate turn-on voltage. If the Schottky barrier of the gate–source junction is turned on, the transconductance g_m rapidly decreases due to the loss in the gate–source junction. Theoretically, the RF drive level for the highest efficiency is the incident power that makes the gate–source barrier turn on, but this level may degrade the active device. Thus, in practical design, it is better to select a level slightly below the theoretical RF drive level.

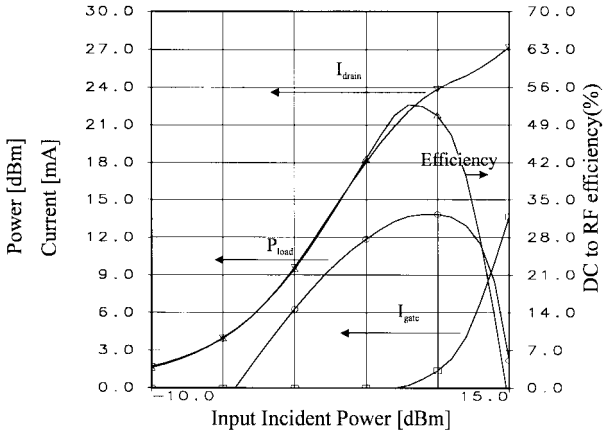


Fig. 5. The ADA results for an analytic harmonic load line of FHX35LG at $V_{\rm GS} = -0.5$ V and $V_{\rm DS} = 2$ V, where $P_{\rm osc}$ and efficiency are calculated from (1) and (2).

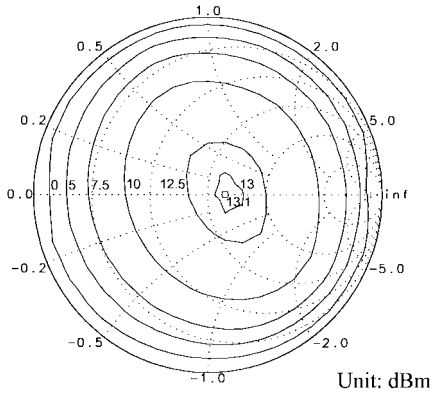


Fig. 6. Output power contours on the Smith chart of the fundamental impedance with the second harmonic terminated with the impedance of (7) ($V_{\rm GS} = -0.65$ V, $V_{\rm DS} = 2$ V and $|V^+_{1,\rm RF}(\omega_o)| = 7$ dBm).

B. Load–Pull Harmonic Load Line for Maximum Power or Highest Efficiency

The output power and efficiency in Fig. 2 depend on the initial dc bias conditions, load impedance, and RF drive level. To investigate the effects of the fundamental frequency load impedance $Z_l(\omega_o)$ on the performance of the oscillator, the load–pull is carried out on the Smith chart of the fundamental impedance with the second harmonic terminated with an impedance of (7). The load impedance can considerably change output power and efficiency, as shown in Figs. 6 and 7. These results are similar to those of power amplifiers. In Figs. 6 and 7, it is noted that the optimum loads of maximum output power and highest efficiency are slightly different. This is due to the variation in the drain current to the load impedance, as shown in Fig. 8. The slight variation of the drain current changes efficiency around the maximum output power. The reflection coefficients calculated from (7) and obtained

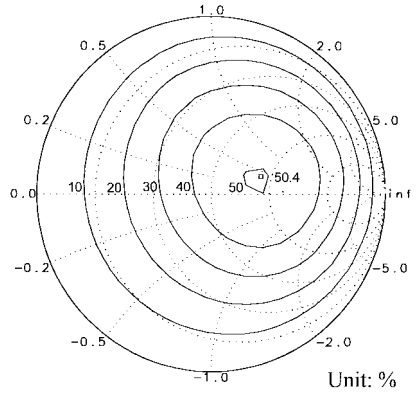


Fig. 7. DC–RF conversion efficiency contours on the Smith chart of the fundamental impedance, where the second harmonic is terminated with the impedance of (7) ($V_{\rm GS} = -0.65$ V, $V_{\rm DS} = 2$ V and $|V^{+}_{1,\rm RF}(\omega_o)| = 7$ dBm).

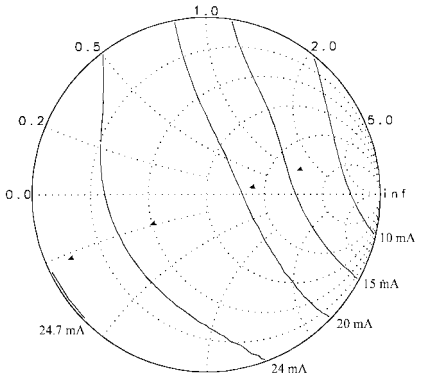


Fig. 8. DC drain-current variation on the Smith chart of the fundamental impedance, where the second harmonic is terminated with the impedance of (7) ($V_{\rm GS} = -0.65$ V, $V_{\rm DS} = 2$ V, and $|V^{+}_{1,\rm RF}(\omega_o)| = 7$ dBm).

from the load–pull for the highest efficiency are

$$\Gamma_l(\omega_o) = \begin{cases} 0.1 + j0.05, & \text{from the analytic harmonic load line of (7)} \\ 0.1 + j0, & \text{from the load–pull of Fig. 6.} \end{cases} \tag{8}$$

The optimum load calculated from the analytic load line is very similar to that of the load–pull. For the circuits initially biased near pinchoff, the harmonic effect on the output power is very important. To examine the harmonic effects, the second harmonic load–pull is performed. As it is known that the output power and efficiency can be improved by selecting a reactive harmonic termination, the second harmonic effects are studied by varying the phase of the second harmonic reflection coefficient for a reactive load. As shown in Fig. 9, the output power of 2.5 dB and the dc-to-RF conversion efficiency of 17.5% can be improved by properly selecting the phase of the second harmonic load in the case of a low gate bias ($V_{\rm gs} = -0.65$ V). In Fig. 9, the point of the best performance corresponds to the shorted load. We also perform the second harmonic source–pull at the same drive level ($|V^{+}_{1,\rm RF}(\omega_o)| = 7$ dBm). The result shows that the performance variation is very small when the second harmonic load is incorporated

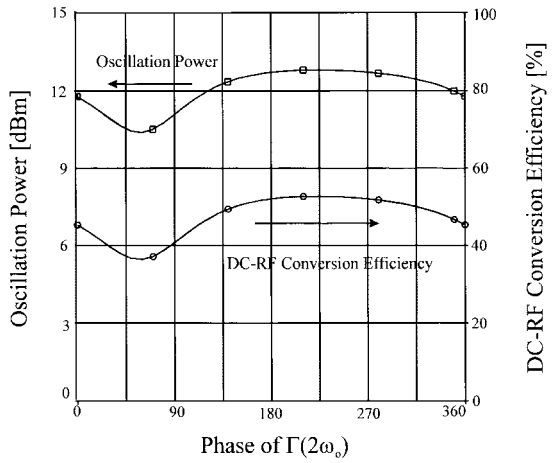
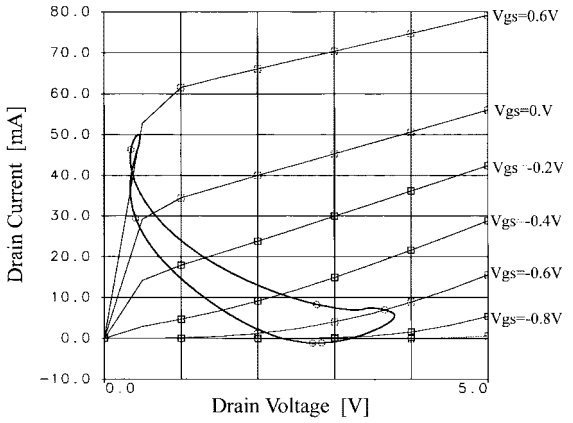
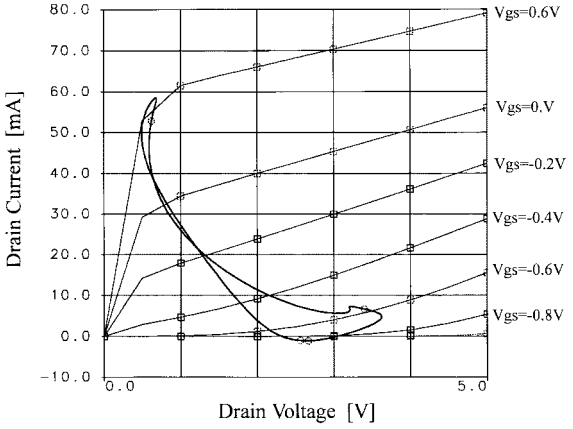


Fig. 9. Output power and dc–RF conversion efficiency with respect to the phase of the second harmonic reflection coefficient ($\Gamma_l(\omega_o) = 0.1 + j0$, $|V^{+}_{1,\rm RF}(\omega_o)| = 7$ dBm, $V_{\rm GS} = -0.65$ V, and $V_{\rm DS} = 2$ V).



(a)



(b)

Fig. 10. Output load lines for (a) maximum efficiency condition ($\Gamma_l(\omega_o) = 0.287\angle 29.25°$, $\Gamma_l(2\omega_o) = 1\angle 225°$) and (b) maximum output power condition ($\Gamma_l(\omega_o) = 0.112\angle 26.56°$, $\Gamma_l(2\omega_o) = 1\angle 225°$) at ($|V^{+}_{1,RF}(\omega_o)| = 7$ dBm, $V_{\rm GS} = -0.65$ V, and $V_{\rm DS} = 2$ V).

at the input port. To the authors' knowledge, this is because the input drive level (7 dBm) is sufficiently lower than the maximum operating point (approximately 10 dBm, as shown in Fig. 5). There should be more power (or efficiency) variations due to input harmonic loads as the input drive level increases.

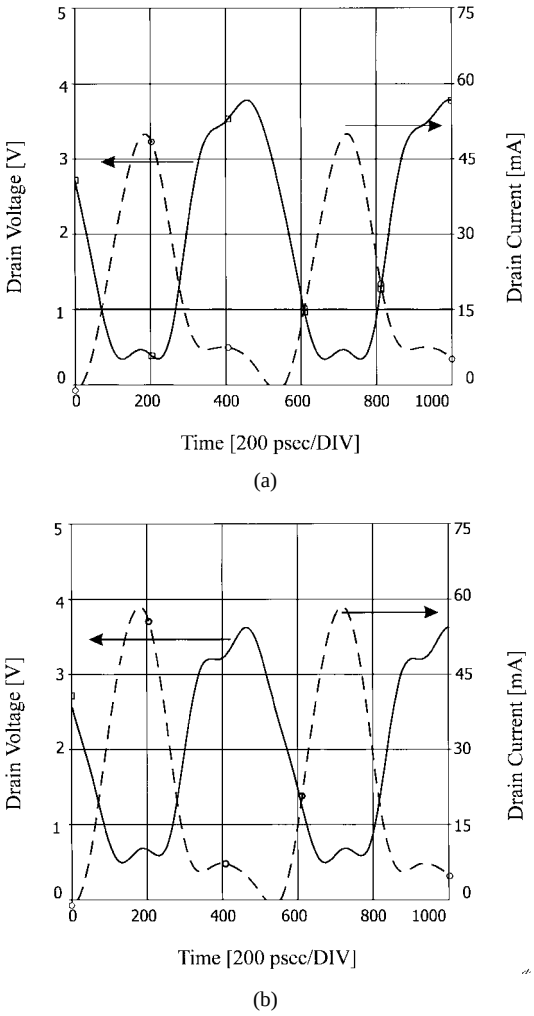


Fig. 11. Voltage and current waveforms at: (a) maximum efficiency condition ($\Gamma_l(\omega_o) = 0.287\angle 29.25^\circ$ and $\Gamma_l(2\omega_o) = 1\angle 225^\circ$) and (b) maximum output power condition ($\Gamma_l(\omega_o) = 0.112\angle 26.56^\circ$ and $\Gamma_l(2\omega_o) = 1\angle 225^\circ$) at ($|V^+_{1,RF}(\omega_o)| = 7$ dBm, $V_{\rm GS} = -0.65$ V, and $V_{\rm DS} = 2$ V).

Fig. 10(a) and (b) shows the load-line curves for maximum efficiency and maximum output power, respectively. Since only the second harmonic component is optimized to be shorted in the above procedure, our oscillator may operate between class-B and class-F. Fig. 11(a) and (b) shows time waveforms of drain voltage and current for maximum efficiency and maximum output power, respectively. They have nearly square waveforms and their waveforms are nearly out of phase, therefore, the dc power consumption becomes quite small.

Fig. 12 shows the simulation results of the output power and dc-to-RF conversion efficiency for the various initial dc bias points. Notice that there is the optimum drain voltage for maximum efficiency at which transconductance is maximum. If the drain voltage increases beyond the optimum value, the output power increases while the efficiency decreases slightly. It is interesting to note that conversion efficiency is not sensitive to the initial dc bias, while the output power is quite dependent on it. The initial bias point has no first-order relationship to the class of operation, but it imposes a limit on the terminal voltages and currents in the oscillator.

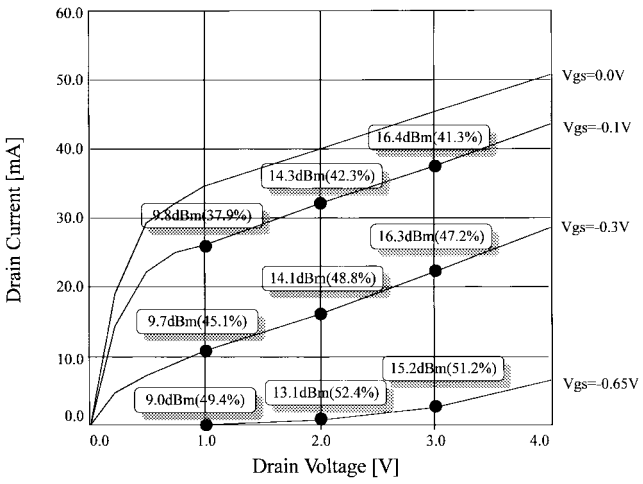


Fig. 12. Maximum output power and maximum efficiency for various initial dc bias points. This simulation is carried out with second harmonic impedance shorted.

IV. Criteria for the Self-Oscillation Condition

As the gate bias goes down near pinchoff, the efficiency of the oscillator is shown to be increased in Fig. 12. However, the transconductance (g_m) of the device is so small near the pinchoff bias that oscillators may have a bad start-up condition. It is necessary to test the oscillation possibility for such a circuit. An oscillation is triggered by noise and builds up until it reaches the steady-state condition. Hence, two conditions—start-up and build-up—are required to test whether or not the designed circuit oscillates at the desired frequency and RF-drive level. The start-up condition is used as a small-signal stability criterion to check whether or not the designed circuit meets the linear (or small-signal) oscillation condition. The build-up condition is used as a large-signal criterion to test whether or not the noise satisfying the linear oscillation condition builds up to the desired RF-drive level.

A. System Characteristic Equation (SCE) as a Small-Signal Criterion for the Start-Up Condition

It is important to check at which frequency the oscillation will start up in response to ambient noise. For this purpose, we have devised a graphical approach that can test whether a linear circuit has an unstable pole near a particular frequency. As a test function, the SCE is considered because it exists uniquely for a linear circuit. An accurate SCE is defined by using node-based parameters, such as Y-parameters, but it is so complex that we cannot quickly assess the stability of a given circuit [11].

In order to test the stability of a circuit more quickly, we define the SCE using the two-port S-parameters of the active transistor and embedding feedback network, as shown in Fig. 13.

Using Mason's rule, the SCE is given by

$$\Delta(p) = 1 - \Sigma L(1) + \Sigma L(2) - \Sigma L(3) + \cdots = 0 \qquad (9)$$

where $\Sigma L(1)$, $\Sigma L(2)$, $\cdots$ are the first- and the second-order loop sums defined in Mason's rule, respectively. The SCE of

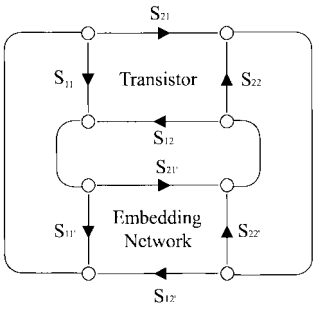


Fig. 13. The representation of a signal-flow graph for the oscillator. S_{ij} and S'_{ij} represent the active transistor and embedding network, respectively.

the general feedback circuit is given by

$$\Delta(p)=1-\left\{S_{11}S'_{11}+S_{21}S'_{12}+S_{22}S'_{22}+S_{12}S'_{21}-|S||S'|\right\}=0 \tag{10}$$

where p is a complex angular frequency, S_{ij}'s are the S-parameters of the transistor, and S'_{ij}'s are that of the feedback network.

The real term of the solution, p of (10) is given by (detailed derivation is given in Appendix II)

$$\sigma = -\Delta(j\omega_o)\mathrm{Im}\left\{\frac{\partial}{\partial\omega}\Delta(j\omega_o)\right\}\Big/\left|\frac{\partial}{\partial\omega}\Delta(j\omega_o)\right|^2. \tag{11}$$

We use the sign of σ as a criterion to test whether a linear circuit is stable or unstable. A positive sign of σ means that a pole of characteristic equation exists in the right half-plane and, therefore, the circuit may oscillate at ω_o. The sign of σ is determined by two factors—$\Delta(j\omega_o)$ and $\mathrm{Im}\{(\partial/\partial\omega)\Delta(j\omega_o)\}$. In many cases, only $\Delta(j\omega_o)$ is used as a criterion for stability, but it is meaningful only if the imaginary part of the derivative of the SCE with respect to frequency is positive. Since S-parameters depend on the normalization impedance, the sign of $\Delta(j\omega_o)$ may be positive or negative. Therefore, the sign of $\Delta(j\omega_o)$ is not sufficient for the decision of stability.

The sign of σ is more easily found using a graphical method. Fig. 14 shows the locus of the SCE of the designed oscillator. Since $\Delta(j\omega_o) < 0$ and $\mathrm{Im}\{(\partial/\partial\omega)\Delta(j\omega_o)\} > 0$, the sign of σ is positive, therefore the designed circuit is unstable and the initial oscillation occurs near $f_o = 1.90$ GHz.

B. Added Power Gain as a Large-Signal Criterion for Build-Up of the Oscillation Condition

At the beginning, the oscillation is triggered by a small-signal noise, after which the triggered signal builds up to the steady-state signal. The amplitude of the input drive voltage of the transistor is varied in the transient process from the start-up to the steady state. In order to investigate the build-up process of the oscillation signal, the gain of transistor and loss of the embedding network should be compared [12] in the transient process since the added power gain is a function of the amplitude of the input drive voltage. At the steady state, the loss of the embedding network should be the same as the added power gain of transistor. The added power gain of a

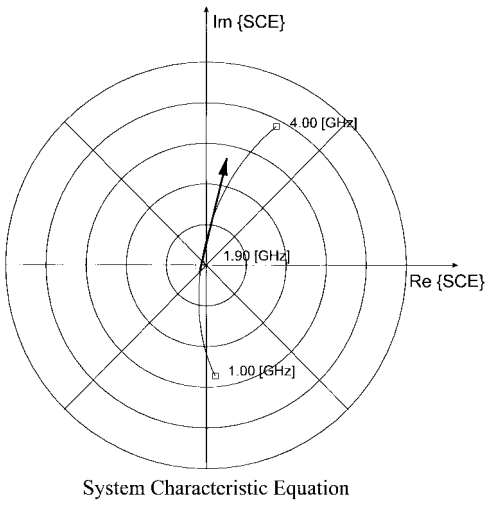


Fig. 14. Graphical illustration of the SCE around the oscillation frequency for the designed oscillator. $\Delta(j\omega_o) < 0$ and $(\partial/\partial\omega)\{\Delta(j\omega_0)\} > 0$, therefore, the designed circuit is unstable and oscillates around ω_o.

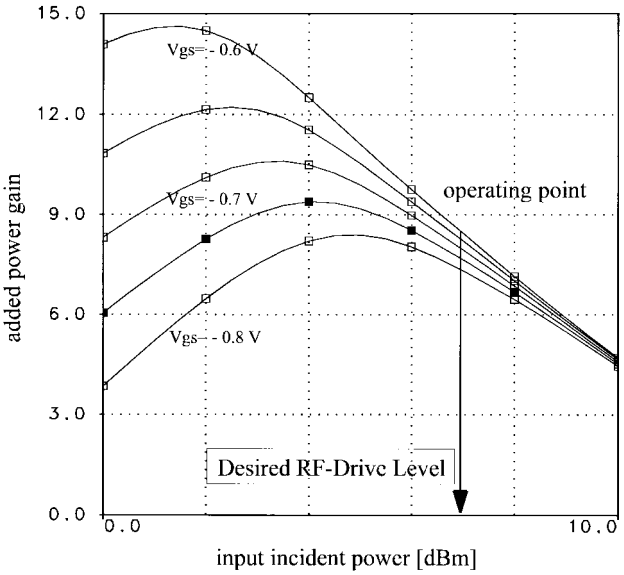


Fig. 15. Curves of added power gain for different V_{GS}'s, which are the results of the ADA ($\Gamma_l(\omega_o) = 0.1\angle 0°$ and $\Gamma_l(2\omega_o) = 1\angle 230°$).

device can be defined as

$$G_{\mathrm{add}}\left(|V_1^+|\right) = \frac{|V_2^-|^2 - |V_2^+|^2}{|V_1^+|^2 - |V_1^-|^2}. \tag{12}$$

In order to reach the desired steady-state oscillation condition, the added power gain at start-up must be larger than that at the steady-state incident power level determined from the analysis of the active device, i.e.,

$$G_{\mathrm{add}}(|V^+_{1,\text{start-up}}|) \geq G_{\mathrm{add}}(|V^+_{1,\text{steady-state}}|), \quad \text{in transient process} \tag{13}$$

where $|V^+_{1,\text{start-up}}|$ is the input drive level at start-up and $|V^+_{1,\text{steady-state}}|$ is the desired RF-drive level at steady state.

The curves of the added power gain for different gate voltages are shown in Fig. 15, where the gains are varied appreciably with the input incident power level. In Fig. 15, if the RF drive level is chosen at the point marked with an arrow,

TABLE I
SPECIFICATION OF HEMT USED IN THE DESIGN

Items	FHX 35 LG
Gate Length	0.25[μm]
Gate Width	280 [μm]
I_{dss}	30 [mA]
$V_{ds,max}$	4.0 [V]
P_{1dB}	14 [dBm]
f_t	35 [GHz]
I_{max}	55.4 [mA]
V_ϕ	0.6 [V]
V_{sat}	0.54 [V]
V_p	-0.55 [V]

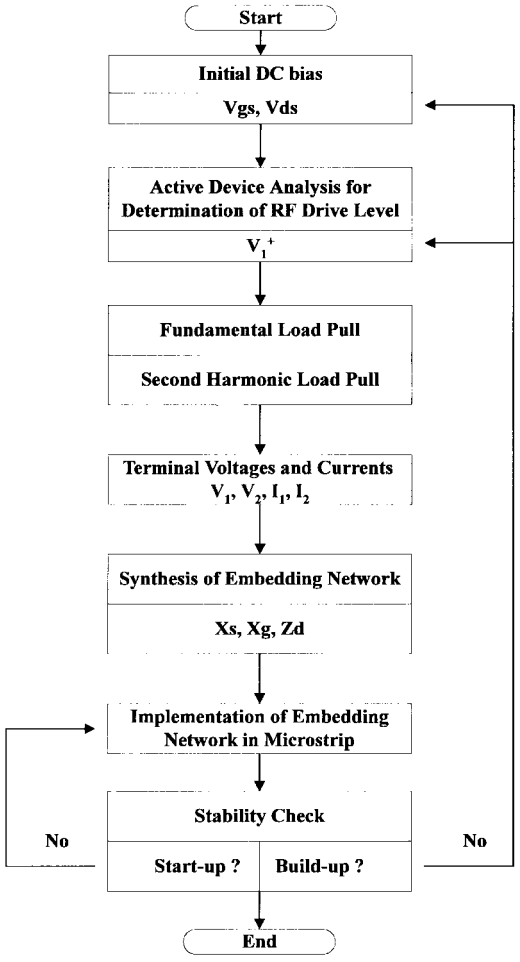


Fig. 16. Flowchart for the design procedure.

oscillators biased with $V_{GS} = -0.6$ V and $V_{GS} = -0.65$ V can reach the designed operation point (the steady-state oscillation condition) because (13) is satisfied. However, the oscillator biased below $V_{GS} = -0.65$ V cannot reach the designed steady state. In this case, the designed circuit cannot oscillate by itself. Thus, in order to design oscillators in the self-oscillating mode, the gate bias voltage should be larger than -0.65 V.

V. OSCILLATOR DESIGN AND PERFORMANCE

The proposed design method is demonstrated by designing a high-efficiency oscillator using a Fujitsu HEMT (FHX35LG) at 1.86 GHz. Table I illustrates the specifications of the HEMT used in this paper. Fig. 16 shows a flowchart to summarize the design procedures mentioned above. To realize the harmonic load in the embedding network, the source impedance is shorted at $2\omega_o$ and then the second harmonic load $\Gamma_l(2\omega_o)$ is synthesized at the drain port. The effects of the second harmonic impedance of the gate impedance, $x_g(2\omega_o)$ is neglected. The implementation of the embedding network is shown in Fig. 17. At drain load, the second harmonic reactive termination is implemented by microstrip lines and radial stubs. An efficiency of 61% is obtained by setting the gate voltage to -1.5 V, which is the maximum efficiency over the entire operating gate voltages. The maximum output of 14.46 dBm is obtained at $V_{gs} = -0.5$ V. Since the 1-dB saturated output power of this device is approximately 14 dBm, the operating point of the HEMT is in a strong saturation region. This RF-drive level makes the gate–source Schottky barrier turn on slightly. The self-oscillation mode is observed when the gate bias voltage is higher than -0.65 V, which shows good agreement with the prediction from (12). Fig. 18 plots efficiency and output power as a function of gate bias. Experimental data agree well with the theoretical prediction by the proposed ADA shown in Table II. Some published high-efficiency oscillator results are compared in Fig. 19. The designed oscillator has the highest efficiency with a low drain bias of 2 V.

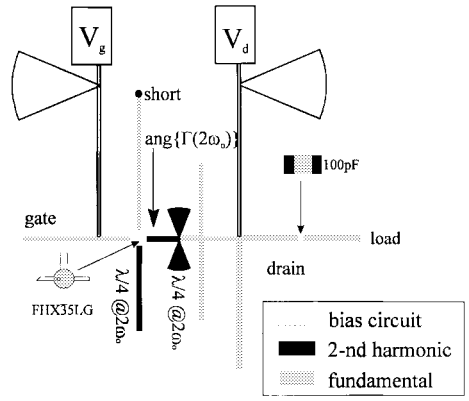


Fig. 17. Circuit layout of the designed high-efficiency harmonic loaded oscillator.

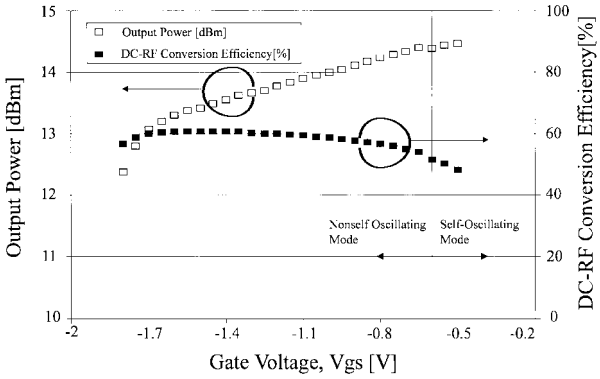


Fig. 18. Experimental results ($V_{DS} = 2$ V and $f_o = 1.86$ GHz).

TABLE II
COMPARISONS OF ADA ANALYSIS AND MEASURED DATA AT: (a) $V_{GS} = -0.5$ V AND $V_{DS} = 2$ V AND (b) $V_{GS} = -0.65$ V AND $V_{DS} = 2$ V

V_{GS}= -0.5 V	Prediction(ADA)	Measured
Output Power	13.62 dBm	14.46 dBm
DC-to-RF Efficiency	51.50 %	48.32 %

(a)

V_{GS}= -0.65 V	Prediction(ADA)	Measured
Output Power	13.58 dBm	14.40 dBm
DC-to-RF Efficiency	52.70 %	53.84 %

(b)

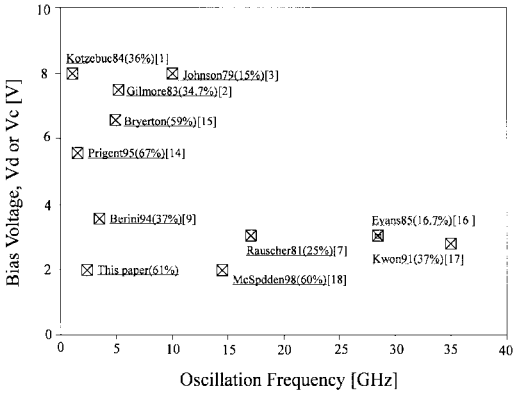


Fig. 19. Reported high-efficiency oscillators.

VI. CONCLUSION

A systematic design method has been presented for the design of a high-efficiency harmonic loaded oscillator. Using the proposed method, output power, efficiency, and dc-bias current shift can be predicted in the design stage by only analyzing the active device. The effects of the fundamental and harmonic loads on dc–RF conversion efficiency and output power was discussed. In the authors' experience, the oscillation analysis in the frequency domain has a severe convergence problem with respect to the position of OSCTEST. However, the proposed approach has rarely the convergence problem since it has the more simple topology than the oscillation circuit. Two stability criteria of start-up and build-up were derived and applied to the design of a high-efficiency oscillator. An HEMT oscillator was built and tested to verify the proposed approach. An efficiency of 61% with a bias of 2 V has been successfully demonstrated at 1.86 GHz. Good agreement has been found between the measured data and prediction from the proposed design approach. This approach has, therefore, been used to effectively optimize the performance of the oscillator.

APPENDIX I
EXTERNAL EMBEDDING CIRCUIT SYNTHESIS

The oscillator circuit can be decomposed into the active and embedding networks, as shown in Fig. 3. The terminal voltages and currents can be expressed in Z-parameters as

$$\begin{pmatrix} V_1^e(\omega_0) \\ V_2^e(\omega_0) \end{pmatrix} = \begin{pmatrix} Z_{11}^e & Z_{12}^e \\ Z_{12}^e & Z_{22}^e \end{pmatrix} \begin{pmatrix} I_1^e(\omega_0) \\ I_2^e(\omega_0) \end{pmatrix} \tag{14}$$

where Z_{ij}^e's $(i, j = 1, 2)$ represent the impedance parameters for the passive embedding network. For the T-shaped embedding network, shown in Fig. 3, the passive embedding network parameters are expressed in terms of the source, gate, and drain impedances of Fig. 3 by

$$Z_{12}^e = Z_s \tag{15}$$

$$Z_{11}^e = Z_g + Z_s \tag{16}$$

$$Z_{22}^e = Z_d + Z_s. \tag{17}$$

By substituting (15)–(17) into (14) and using the terminal voltages and currents, the elements of the embedding network are arranged by

$$\begin{pmatrix} Z_g \\ Z_d \end{pmatrix} = -\begin{pmatrix} V_1/I_1 & 1 + I_2/I_1 \\ V_2/I_2 & 1 + I_1/I_2 \end{pmatrix} \begin{pmatrix} 1 \\ Z_s \end{pmatrix} \tag{18}$$

where $V_1 = V_1^e$, $V_2 = V_2^e$, $I_1 = -I_1^e$ and $I_2 = -I_2^e$ are used.

For a simple expression of (18), we introduce the following four variables:

$$z_1 = -\frac{V_1}{I_1} \tag{19}$$

$$z_2 = -\frac{V_2}{I_2} \tag{20}$$

$$\beta_f = -(1 + A_I) = -\left(1 + \frac{I_2}{I_1}\right) \tag{21}$$

$$\beta_b = -\left(1 + \frac{1}{A_I}\right) = -\left(1 + \frac{I_1}{I_2}\right) \tag{22}$$

where $A_I = I_2/I_1$.

Using (19)–(22), (18) can be rewritten as

$$\begin{pmatrix} Z_g \\ Z_d \end{pmatrix} = \begin{pmatrix} z_1 & \beta_f \\ z_2 & \beta_b \end{pmatrix} \begin{pmatrix} 1 \\ Z_s \end{pmatrix}. \tag{23}$$

For a specific case in which the load is connected to the drain port, the source and gate impedances are set by a purely lossless element, i.e., $Z_s = jx_s$ and $Z_g = jx_g$. The elements of the embedding network can be evaluated by

$$Z_d = z_2 + j\beta_b \frac{\mathrm{Re}\{z_1\}}{\mathrm{Im}\{\beta_f\}} \tag{24}$$

$$jx_s = j\frac{\mathrm{Re}\{z_1\}}{\mathrm{Im}\{\beta_f\}} \tag{25}$$

$$jx_g = j\mathrm{Im}\{z_1\} + j\mathrm{Re}\{\beta_f\}\frac{\mathrm{Re}\{z_1\}}{\mathrm{Im}\{\beta_f\}}. \tag{26}$$

APPENDIX II
SMALL-SIGNAL STABILITY CRITERION FOR THE START-UP CONDITION

It is assumed that the solution p of (9) is located near the zero phase frequency of Δ on the $j\omega$ axis defined by

$$\Phi\Big[\Delta(j\omega_0)\Big] = 0. \tag{27}$$

It is convenient to write the solution p of (9) as

$$p = j(\omega_0 + \delta\omega) + \sigma \tag{28}$$

where $\delta\omega$ and σ are assumed to be small relative to ω_o.

TABLE III
FOUR CASES OF STABILITY

$\Delta(j\omega_o)$	$Im\{\frac{\partial}{\partial\omega}\Delta(j\omega)\}$	Stability Criterion
$\Delta(j\omega_o)>0$	$Im\{\frac{\partial}{\partial\omega}\Delta(j\omega)\}>0$	Stable
$\Delta(j\omega_o)>0$	$Im\{\frac{\partial}{\partial\omega}\Delta(j\omega)\}<0$	Unstable
$\Delta(j\omega_o)<0$	$Im\{\frac{\partial}{\partial\omega}\Delta(j\omega)\}>0$	Unstable
$\Delta(j\omega_o)<0$	$Im\{\frac{\partial}{\partial\omega}\Delta(j\omega)\}<0$	Stable

The SCE of (9) can be rewritten by the Taylor expansion around ω_o so that

$$\Delta(p)\approx\Delta(j\omega_0)-\frac{\partial}{\partial\omega}\Delta(j\omega)\bigg|_{\omega=\omega_0}(\delta\omega-j\sigma)=0. \quad (29)$$

Splitting (29) into real and imaginary parts, equations for $\delta\omega$ and σ are obtained by

$$\text{Real}: \ \Delta(j\omega_0)-\Delta^r_\omega\delta\omega-\Delta^i_\omega\sigma=0 \quad (30)$$

$$\text{Imag}: \ \Delta^r_\omega\sigma-\Delta^i_\omega\delta\omega=0 \quad (31)$$

where Δ^r_ω and Δ^i_ω represent the real and imaginary parts of the partial derivative of Δ with respect to ω, respectively. Solving for σ with (30) and (31) gives

$$\sigma=-\Delta(j\omega_0)\text{Im}\left\{\frac{\partial}{\partial\omega}\Delta(j\omega_0)\right\}\Big/\left|\frac{\partial}{\partial\omega}\Delta(j\omega_0)\right|^2. \quad (32)$$

If the sign of σ is positive, the system pole of (9) exists in the right-hand-side plane. This means that the circuit may oscillate at $\omega_o+\delta\omega$. The sign of σ is determined by two factors: $\Delta(j\omega)$ and $(\partial/\partial\omega)\{\Delta(j\omega_0)\}$. Four cases for stability are listed in Table III.

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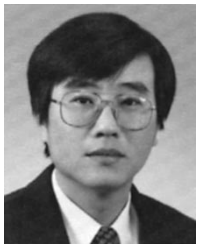

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