A CMOS Outphasing Power Amplifier With Integrated Single-Ended Chireix Combiner

Sungho Lee, *Student Member, IEEE*, and Sangwook Nam, *Member, IEEE*

***Abstract*—This brief proposes an on-chip outphasing power amplifier that uses a single-ended Chireix combiner for a linear amplification with a nonlinear component amplifier. The proposed combiner structure consists of a lumped inductor and a lumped capacitor that can achieve the simple single-ended configuration of a Chireix combiner. It is also suitable for on-chip implementation with minimum efficiency deterioration. An inductance–capacitance balun using the lumped model of $\lambda/4$ and $3\lambda/4$ transmission lines was effectively merged into a simple Chireix combiner for two outphased input signals. The relation between the output resistance and the outphasing angle of the input signals was derived to determine the maximum efficiency. A voltage-mode class-D power amplifier was used with the combiner to illustrate the combiner's effectiveness. The prototype fabricated in a 0.13-μm complementary metal–oxide–semiconductor process shows a maximum 52% power-added efficiency (continuous wave) and a -47-dBc adjacent channel power ratio performance at a 10-MHz offset with a 1.92-GHz wideband code-division multiple-access signal.**

***Index Terms*—Complementary metal–oxide–semiconductor (CMOS) power amplifier (PA), outphasing PA, single-ended Chireix combiner.**

I. Introduction

WIRELESS communication, now omnipresent, makes battery lifetime particularly critical to maintain the multiple functions of today's mobile equipment. To achieve long operating times for handheld equipment, many studies have focused on the structure of the power amplifier (PA), the main source of power consumption in most transmitters. One potential solution is an outphasing amplifier, as proposed by Chireix [1]. The outphasing amplifier consists of an AM–PM modulator, two highly efficient nonlinear amplifiers, and a power combiner. It is one of the candidates for a highly efficient PA. In an outphasing amplifier, an input signal containing both AM and PM is divided into two constant envelope phase-modulated signals by an AM–PM modulator, and then two amplified signals created by highly efficient nonlinear amplifiers are summed by a passive power combiner [2], [3]. In the conventional outphasing amplifiers shown in Fig. 1(a) and (b), the maximum output power is obtained when the two signals are combined with phase differences of 180° and 0°, respectively.

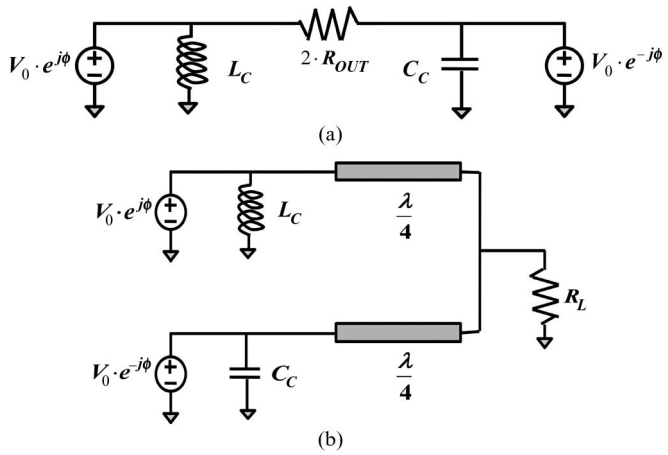

Fig. 1. Conventional structure of a Chireix combiner. (a) Basic structure and (b) typical single-ended configuration using transmission lines.

The design of the combiner is critical because it affects the overall efficiency of the outphasing amplifiers. There are two kinds of power combiners, and each has merits and demerits. For a matched combiner such as the Wilkinson combiner, the out-of-phase component of two constant phase-modulated signals is dissipated in the isolation resistor of the combiner. Hence, this method leads to a waste of power and degradation of the efficiency for a high peak-to-average power ratio signal. On the other hand, nonisolated combiners, such as transformers and LC baluns, provide phase-varying impedances to PAs. The dc power consumption will vary according to the load impedance if the PAs act as ideal low-impedance sources, and the phase-varying impedances are properly controlled. However, when the transformer or LC balun is integrated into a chip in a lossy medium such as a CMOS process, power losses are severe due to the weak magnetic coupling and the low-quality factors of the passive components. Also, the chip area will be increased. Hence, it is important to reduce the number of inductors.

Previously, Chireix combiners used additional inductors or a transformer to convert a differential-to-single output, which

Manuscript received July 3, 2009; revised October 22, 2009 and January 22, 2010; accepted February 6, 2010. Date of publication May 27, 2010; date of current version June 16, 2010. This work was supported by the Korea Science and Engineering Foundation through the National Research Laboratory Program funded by the Ministry of Science and Technology [ROA-2007-000-20118-0(2007)]. This work was recommended by Associate Editor J. Buckwalter.

S. Lee is with the Applied Electromagnetics Laboratory, School of Electrical Engineering and Computer Science, Institute of New Media and Communications, Seoul National University, Seoul 151-742, Korea, and also with the Korea Electronics Technology Institute, Seongnam 463-816, Korea (e-mail: slee@ael.snu.ac.kr).

S. Nam is with the Applied Electromagnetics Laboratory, School of Electrical Engineering and Computer Science, Institute of New Media and Communications, Seoul National University, Seoul 151-742, Korea.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSII.2010.2048353

makes on-chip integration difficult [4], [5]. This brief presents a single-ended outphasing PA using an on-chip integrated Chireix combiner. The proposed combiner simplifies the output configuration of the outphasing PA and minimizes the power loss. In the following sections, the design procedure and the validity of the proposed structure will be described and verified.

II. Single-Ended Chireix Combiner Analysis

A. Conventional Chireix Combiner and LC Balun

A conventional Chireix combiner, as shown in Fig. 1(a), uses an extra inductor L_C and capacitor C_C to compensate for the phase-varying reactance at a given phase difference. Therefore, the PAs can obtain maximum efficiency at a lower power in addition to the peak power. The output power with the maximum efficiency can be selected by the particular choice of the outphasing angle ϕ_c of the two branch signals.

When the highest efficiency occurs, the values of the capacitance and the inductance are determined from the following expressions in terms of the compensated outphasing angle ϕ_c [6]:

$$C_C = \frac{1}{\omega_0}\frac{\sin 2\phi_c}{2R_{\rm OUT}} \tag{1}$$

$$L_C = \frac{1}{\omega_0}\frac{2R_{\rm OUT}}{\sin 2\phi_c}. \tag{2}$$

In (1) and (2), $R_{\rm OUT}$ is the output resistance of the PA, and ω_0 represents the operating fundamental frequency. Since the Chireix combiner shown in Fig. 1(a) is designed for a differential load, a differential-to-single conversion is needed for a single-ended load such as a monopole antenna. The conversion process requires additional passive components, which results in a lower output power and efficiency. To configure a single-ended output, two $\lambda/4$ transmission lines can be used as a combiner, as shown in Fig. 1(b) [4]. This structure offers good efficiency when the amplifier is backed off from maximum output power. The main drawback of this combiner is its large physical size. To avoid the drawback, the combiner can be implemented using lumped element circuits equivalent to the $\lambda/4$ transmission line [5]. However, this uses too many inductors, which complicates the output configuration and deteriorates the efficiency.

B. Proposed Single-Ended Chireix Combining Technique

In this brief, we utilized a lumped component balun based on $\lambda/4$ and $3\lambda/4$ transmission, as shown in Fig. 2(a). The $\lambda/4$ transmission line can be modeled by one inductor and two capacitor components. The characteristic impedance is expressed as the ratio of the inductance and the capacitance. In a similar manner, the $3\lambda/4$ transmission line can also be modeled by two inductors and one capacitor. This balun achieves the maximum output power when the input signals are antiphase, which is the same as the case in Fig. 1(a). In this study, we implemented a single-ended Chireix combiner by using $C_M - L_M - C_M$ and $L_M - C_M - L_M$ (LC balun, specifically) circuits equivalent to the $\lambda/4$ and $3\lambda/4$ transmission lines, as shown in Fig. 2(b). As 50 Ω is usually designed as the input impedance of antennas, the load impedance R_L was set to 50 Ω. The input admittance

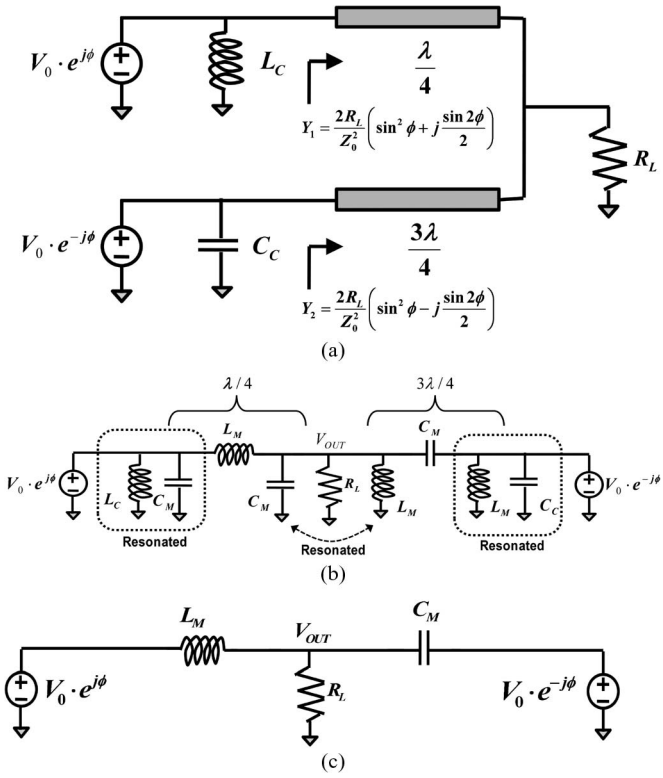

Fig. 2. (a) Proposed configuration using transmission lines. (b) Merged Chireix combiner with balun. (c) Proposed simplified single-ended Chireix combiner.

looking into the $\lambda/4$ and $3\lambda/4$ transmission lines can be obtained by

$$Y_{1,2} = \frac{2R_L}{Z_0^2}\left(\sin^2\phi \pm j\frac{\sin 2\phi}{2}\right). \tag{3}$$

It can also be seen that the compensating reactances are the same as those of the conventional Chireix combiner given by (1) and (2) when $Z_0^2/(2R_L) = R_{\rm OUT}$ and $\phi = \phi_c$.

Using (3), the characteristic impedance of the quarter-wave transmission line is the geometric mean of R_L and the output impedance $R_{\rm OUT}$ as shown in the following:

$$Z_0 = \sqrt{2R_L \cdot R_{\rm OUT}} = \sqrt{\frac{L_M}{C_M}} \tag{4}$$

where $L_M = Z_0/\omega_0$, and $C_M = 1/(Z_0\omega_0)$ is used for the transmission line. Also, the relation between the operating frequency and the components in the LC balun is given by $\omega_0 = 1/(L_M C_M)^{1/2}$ [7].

In Fig. 2(b), L_M and C_M (indicated by the dotted line), parallel to R_L, can be resonated at the operating frequency. The L_C used in the Chireix combiner and the C_M used in the modeling of the $\lambda/4$ transmission line are imposed to be resonated at the operating frequency. C_C and L_M work the same (as indicated by the dotted box line). Hence, the resonance condition is given by

$$\omega_0 = \frac{1}{\sqrt{L_M \cdot C_C}} = \frac{1}{\sqrt{L_C \cdot C_M}}. \tag{5}$$

Using (5) with (1) and (2) gives the relation between the outphasing angle of the input signal with the maximum

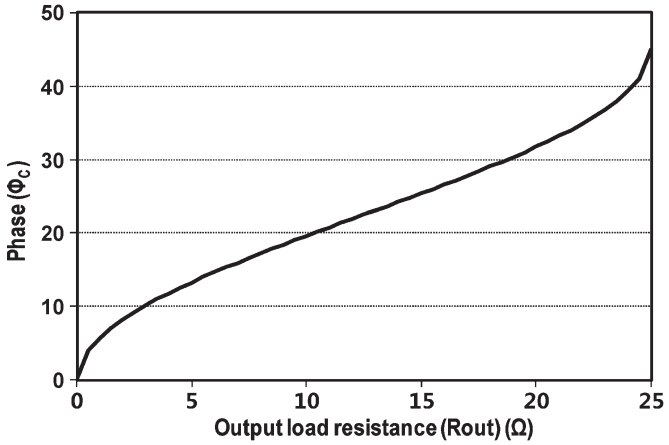

Fig. 3. Relation between output resistance and the input signal's phase for maximum efficiency.

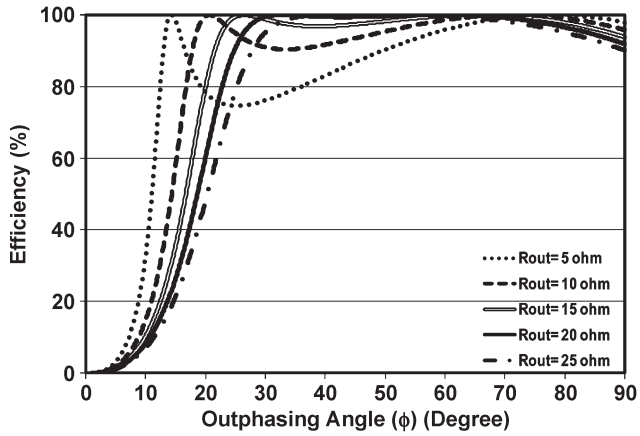

Fig. 4. Simulated efficiency versus the outphasing angle of the proposed combiner.

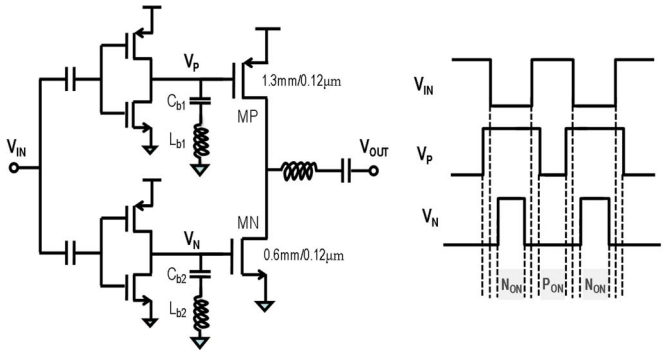

Fig. 5. Schematic and operation of the voltage-mode class-D PA.

efficiency and the output resistance in resonance. It is given by

$$\sin 2\phi_C = \sqrt{\frac{2R_{\rm OUT}}{R_L}} = 0.2\sqrt{R_{\rm OUT}}. \tag{6}$$

Removing all the resonant inductor and capacitor pairs, the structure of the simplified Chireix combiner can be seen in Fig. 2(c). The inductance and the capacitance are expressed by the following:

$$L_M = \frac{\sqrt{2R_L R_{\rm OUT}}}{\omega_0} = \frac{10 \cdot \sqrt{R_{\rm OUT}}}{\omega_0} \tag{7}$$

$$C_M = \frac{1}{\omega_0 \cdot \sqrt{2R_L R_{\rm OUT}}} = \frac{0.1}{\omega_0 \cdot \sqrt{R_{\rm OUT}}}. \tag{8}$$

From (6), we notice that the maximum value for output resistance $R_{\rm OUT}$ is limited to 25 Ω. Therefore, the proposed method is valid for PAs with an $R_{\rm OUT}$ under 25 Ω. However, this limitation on the output resistance is not a problem since the output resistance in PAs is usually a few ohms for high output power. As a result, a single-ended Chireix combiner is achieved by using one capacitor and one inductor with properly selected values. The output power can be derived from Fig. 2(c) for an arbitrary outphasing angle ϕ, as shown in the following:

$$P_{\rm OUT} = \frac{2V_O^2 R_L}{\omega_0^2 L_M^2} \cdot \sin^2 \phi. \tag{9}$$

Fig. 3 shows the graph of the outphasing angle of the maximum efficiency versus the output resistance $R_{\rm OUT}$ given by (6). In Fig. 3, the phase that corresponds to the output resistance indicates that the output resistance determines the phase of the input signal ϕ_c, where the maximum efficiency occurs. For example, when the output resistance is 10 Ω, the maximum efficiency in the Chireix combiner occurs at the outphasing angle of 19.6° in the outphasing amplifier structure. Fig. 4 shows the circuit-level simulation results of the efficiency curves according to various input outphasing angles when the ideal input voltage sources and the combiner with ideal components are used. With a single-ended output configuration, the efficiency curve is the same as the conventional Chireix combiner [8]. However, the maximum efficiency point depends on the value of $R_{\rm OUT}$. As the output resistance decreases, the maximum efficiency point will be shifted to the small input power. However, with smaller output resistance, the degree of the efficiency-curve undershooting is increased. Therefore, the output resistance should be decided by taking the output power and the undershooting efficiency characteristics into account. The limitations of this approach are the dependence of the input outphasing angle on the output resistance and the bandwidth reduction for the maximum efficiency. The −1-dB bandwidth of the proposed combiner is 300 MHz, whereas that of the conventional $\lambda/4$ combiner is 400 MHz at the center frequency of 2 GHz. However, 300 MHz seems to be large enough for cellular wireless applications.

III. Implementation of the Outphasing Amplifier

For ideal Chireix combining, the amplifier should operate in voltage mode. Therefore, we used a class-D PA instead of an overdriven class-B amplifier. To reduce shoot-through current, we controlled the overlapped time of the turn-on time between P-type MOS and N-type MOS during transition by sizing at the driver stage [9]. However, the sizing makes the output pulse of the driver narrow, which requires fast charging and discharging at the input of the last stage (the gate ports of the transistors MP and MN). Since the transistor size of the output stage is usually very large in order to drive low impedance, the fast charging and discharging operation needs a high capacitive driver, which induces large power consumption. Practically, to drive the large gate capacitance of the transistors MP and MN in Fig. 5, the driver's transistor size should be large. This degrades power-added efficiency (PAE) performance. Therefore,

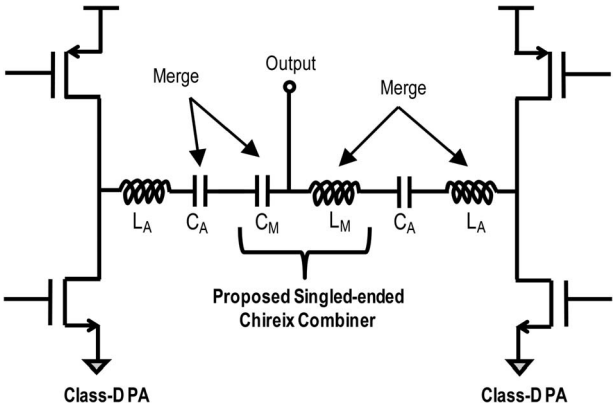

Fig. 6. Merged Chireix combiner with class-D PAs.

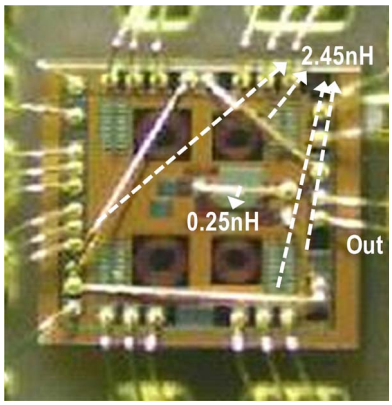

Fig. 7. Chip microphotograph.

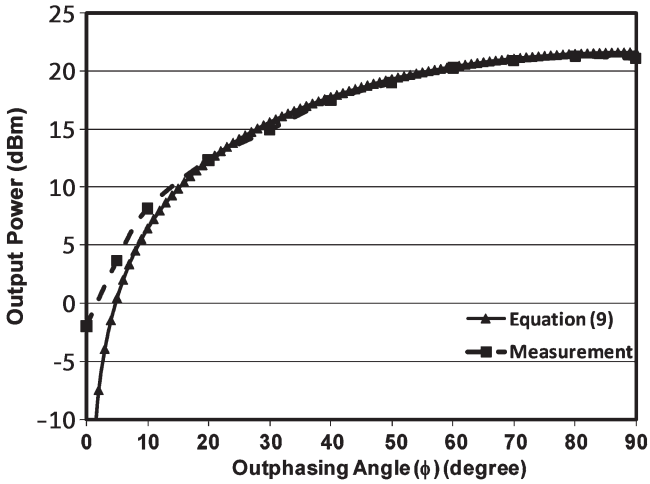

Fig. 8. Measured output power versus the outphasing angle using the CW signal.

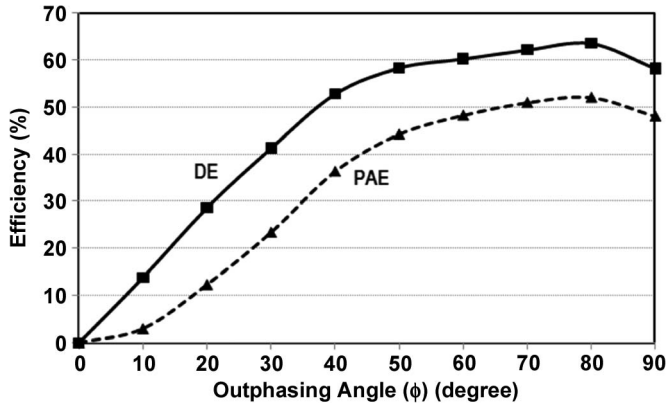

Fig. 9. Measured efficiency versus the outphasing angle using the CW signal.

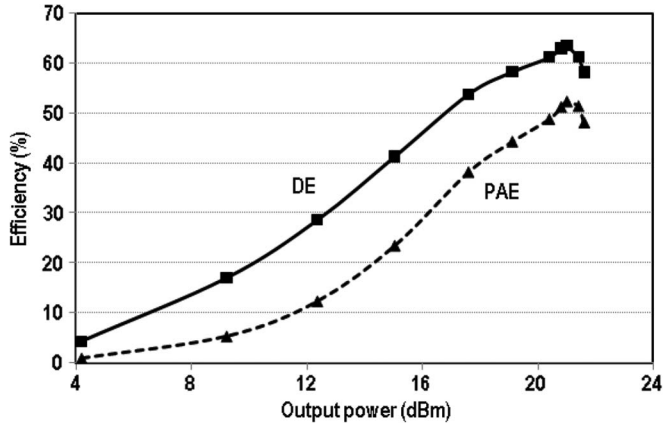

Fig. 10. Measured efficiency versus the output power using the CW signal.

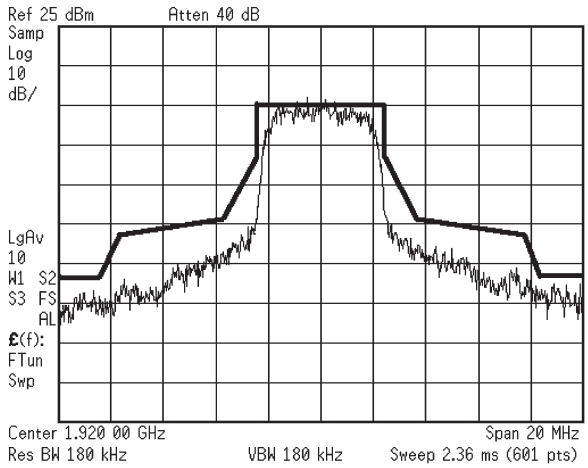

Fig. 11. Measured PA output spectrum with a WCDMA signal.

additional inductors were adopted in this work. The inductors L_{b1} and L_{b2} are resonated capacitance at the gate node at the operating frequency. The capacitors C_{b1} and C_{b2} are also needed for dc blocking. The quality factor of the inductor is not critical because the inductor does not provide a signal path; it simply reduces the capacitance loading effect. By adding the inductors, power consumption at the driver stage can be largely reduced, which increases total system PAE performance. In the simulation, the power consumption at the driver stage was reduced by half with the same driving capability.

Fig. 6 shows the merged Chireix combiner schematic with class-D PAs. One inductor L_M and one capacitor C_M are connected between two class-D amplifiers. The output impedance was set to 7 Ω, which was chosen to optimize the structure's output power and the efficiency. The inductor and the capacitor expressed in (7) and (8) are 2.2 nH and 3.1 pF, respectively. The series LC resonator used at the output of the class-D amplifier is 0.25 nH and 27.5 pF. C_A and C_M can be merged into one capacitor, which becomes 2.8 pF. The inductors L_M and L_A can also be merged in the same way, becoming 2.45 nH.

TABLE I
PERFORMANCE COMPARISON

	Structure	Output Power	Technology	Modulated Signal	PAE (CW)	PAE (WCDMA)	Note
Ref. [9]	LINC	20 dBm	0.18μm CMOS	900MHz CMDA	42%	.	Off-chip Chireix Combiner
Ref. [10]	Polar	27.8 dBm	0.18μm CMOS	900MHz WCMDA	34%	26.50%	external balun
Ref. [11]	Polar	25.2 dBm	0.13μm CMOS	1.92GHz WCDMA	47.60%	38.20%	external balun
This Work	LINC	21.6 dBm	0.13μm CMOS	1.92GHz WCDMA	52%	36%	Integrated single-ended Chireix combiner using bondwires

By this reduction, the number of total inductors can be reduced to six, thus minimizing the inductor area. To utilize the effect of the relatively high-quality factor of the bondwire inductor, in this design, pad-to-pad bondwires were used for the two inductors in the combiner: the small inductor L_A and the large inductor merged by L_A and L_M. The curvature and the height of the bondwires were carefully controlled to obtain accurate inductance. According to electromagnetic simulations, the estimated quality factor of the 2.45-nH bondwired inductor was about 14.

The proposed single-ended Chireix combiner in the outphasing amplifier conducts as an impedance transformer, as well as a differential-to-single converter. As a result, there is no need to add external components for impedance matching. The operation of the voltage-mode class-D amplifier is stable over varying output impedance.

IV. MEASUREMENT RESULTS

The outphasing amplifier with the proposed single-ended Chireix combiner was fabricated in a standard 0.13-μm CMOS process. Fig. 7 shows the microphotograph of the prototype, which occupies an area of 1.0 $\times$ 1.0 mm, including pads. Two class-D PAs are located on the upper and lower sides of the chip. LC series resonators and the proposed combiner were placed at the center of the chip. The series bonding wires were used for 2.45 nH and one short bonding wire for 0.25 nH. For the measurements, we connected the output to a spectrum analyzer directly without having any component on the test board. No external components were used, excluding dc stabilizing capacitors at the supply ports. Two signals were generated from the radio frequency and in-phase quadrature synchronized two Agilent 4438C signal generators.

Fig. 8 shows the output power according to the outphasing angle variation. The theoretical result calculated by (9) matches the measured output power closely. Figs. 9 and 10 show the measured drain efficiency (DE) and PAE performance according to the outphasing angle and output power, when a continuous-wave (CW) signal was applied. A maximum of 64% DE and 52% PAE were obtained when the output power was 21.6 dBm with a 1.9-V supply voltage. The difference between the theoretical and measured curves (Figs. 4 and 9) is thought to be due to the assumption of the ideal low-impedance source and lossless combiner in the simulation of Fig. 4.

The maximum power gain was 14.6 dB. The PA input was configured to maximize voltage swing. Fig. 11 shows the spectrum using a 1.92-GHz modulated signal with a wideband code-division multiple-access (WCDMA) spectrum mask. The adjacent channel power ratio at the 10-MHz frequency offset was -47 dBc when the modulated output power was 17.1 dBm at a 4.5-dB back-off. At the output power, the measured DE and PAE were 51% and 36%, respectively. Table I shows a performance comparison with the other PAs using similar technology. While the output power of the proposed PA is lower, the efficiency is higher for CW sources [10], [11]. The output power and efficiency can be expected to further improve through the use of transistors for high voltage or reduced gate-length transistors supporting rapid operation.

V. CONCLUSION

This brief has presented the first outphasing PA with an on-chip integrated single-ended Chireix combiner using bondwire inductors. The combiner simplifies the output configuration of the outphasing PA and reduces the number of passive components. The adopted voltage-mode class-D amplifier aids the operation of the Chireix combiner, resulting in high efficiency with reduced shoot-through currents. The prototype shows a maximum of 64% DE and 52% PAE at a 1.92-GHz CW signal. With these results, we confirm that the proposed architecture can facilitate the on-chip integration of a PA with minimal efficiency deterioration.

REFERENCES

[1] H. Chireix, "High power outphasing modulation," *Proc. IRE*, vol. 23, no. 11, pp. 1370–1392, Nov. 1935.
[2] S. C. Cripps, *RF Power Amplifier for Wireless Communication*. Boston, MA: Artech House, 1999.
[3] F. H. Raab, "Efficiency of outphasing RF power-amplifier system," *IEEE Trans. Commun.*, vol. COM-33, no. 2, pp. 1094–1099, Oct. 1985.
[4] I. Hakala, D. K. Choi, L. Gharavi, N. Kajakine, J. Koskela, and R. Kaunisto, "A 2.14 GHz Chireix outphasing transmitter," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 6, pp. 2129–2137, Jun. 2005.
[5] J. Gründlingh, K. Parker, and G. Rabjohn, "A high efficiency Chireix outphasing power amplifier for 5 GHz wlan applications," in *Proc. IEEE MTT-S Int. Microw. Symp.*, Fort Worth, TX, Jun. 2004, pp. 1535–1538.
[6] S. Moloudi, K. Takinami, M. Yousself, M. Mikhemar, and A. Abidi, "An outphasing power amplifier for a software-defined radio transmitter," in *Proc. ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 568–569.
[7] P. H. Smith, *Electronic Applications of the Smith Chart*, 2nd ed. Atlanta, GA: Noble, 1995.
[8] X. Zhang, L. E. Larson, and P. M. Asbeck, *Design of Linear RF Outphasing Power Amplifiers*. Norwood, MA: Artech House, 2003, pp. 142–145.
[9] T. Hung, D. K. Choi, L. E. Larson, and P. M. Asbeck, "CMOS outphasing class-D amplifier with Chireix combiner," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 8, pp. 619–621, Aug. 2007.
[10] A. Shameli, A. Safarian, A. Rofougaran, M. Rofougaran, and F. De Flaviis, "A two-point modulation technique for CMOS power amplifier in polar transmitter architecture," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 1, pp. 31–38, Jan. 2008.
[11] C. D. Presti, F. Carrara, A. Scuderi, P. M. Asbeck, and G. Palmisano, "A 25-dBm high-efficiency digitally-modulated CMOS power amplifier for WCDMA/EDGE/OFDM with adaptive digital predistortion and efficient power control," *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp. 1883–1896, Jul. 2009.