A 29 dBm CMOS Class-E Power Amplifier with 63% PAE Using Negative Capacitance

Yonghoon Song, Sungho Lee, Jaejun Lee, Sangwook Nam

INMC, School of Electrical Engineering and Computer Science, Seoul National University, Seoul, Korea

Abstract – **This paper proposes class-E power amplifier including negative capacitance to optimize shunt drain capacitance. The negative capacitance improves efficiency, compensates for surplus shunt drain capacitance resulting from parasitic capacitance, and is implemented without an external circuit. A cascode single-ended class-E RF power amplifier including driver stage is fabricated using a 0.13-µm standard CMOS technology delivering 29 dBm with 66% drain efficiency and 63% power-added efficiency at 1.8 GHz.**

I. Introduction

Mobile wireless equipment requires a high-efficiency RF transmitter to extend battery life span. The power amplifier (PA) is the most critical component in a transmitter, because it consumes the largest portion of the DC power and determines the transmitter's overall efficiency. A class-E PA, highly efficient and simple, is adaptable for a high-efficiency transmitter and has been implemented on CMOS for its low cost [1]-[5].

Nonetheless, driving high currents to deliver large output power and reducing on-resistance of the transistor forced RF designers to widen gate width, a few millimeters in CMOS technology [1]-[4]. However, widening gate width contains undesired parasitic components and increases parasitic drain capacitance. It disturbs class-E operation affecting to shunt drain capacitance C_P (critical value to determine lossless class-E operation depicted in Fig. 1) deviating from optimum value and resulting in efficiency degradation. Furthermore, cascode topology, strengthening reliability from breakdown voltage swing, makes the parasitic capacitance worse on drain capacitance [2].

To solve the efficiency reduction caused by C_P increasing, parasitic drain capacitance must be tuned out. A shunt inductor with DC block capacitance might be inserted on the same node on C_P, thus tuning out parasitic drain capacitance [3]. However, the inductor requires a large area to integrate on a chip and the inductor contains parasitic capacitance in itself.

In this paper, we proposed a cascode class-E PA using negative capacitance to tune out parasitic capacitance without adding external circuits. In CMOS technology, a capacitor usually uses smaller area containing less parasitic components than does an inductor. We present a cascode class-E PA that delivers 29 dBm with 63% power-added efficiency (PAE) at 1.8 GHz using a 0.13-µm standard CMOS process.

II. Class-E Shunt Capacitance Analysis

Fig. 1 shows the basic schematic of a CMOS class-E amplifier. For the lossless class-E operation mode, it is necessary to provide the hard switching operation and zero

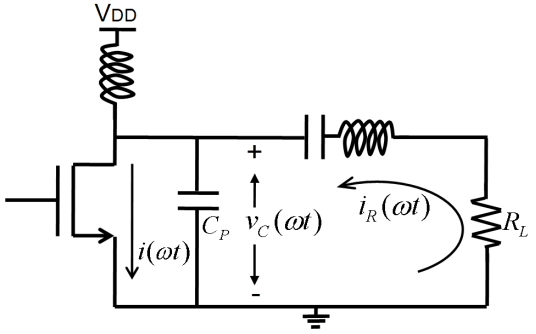

Fig. 1. Basic class-E amplifier schematic.

voltage switching (ZVS) [6]. When transistor is off for $\pi \le \omega t < 2\pi$, $v_C(\omega t)$ can be written as below [7],

$$v_C(\omega t) = -\frac{I_R}{\omega C_P}[\cos(\omega t + \varphi) + \cos\varphi + (\omega t - \pi)\sin\varphi] \quad (1)$$

where I_R represents the magnitude of $i_R(\omega t)$, in Fig. 1. When (1) satisfies the ZVS condition at $\omega t = 2\pi$, $\varphi = -0.18\pi$ radian and $\omega C_P R_L = 0.1836$ are determined avoiding the overlapping of waveforms $v_C(\omega t)$ and i_R in Fig. 1 [8].

However, in the real world, C_P variation exists on class-E CMOS PA from parasitic capacitance or process variation. Thus, the $\omega C_P R_L$ value cannot maintain 0.1836 with fixed R_L at given frequency. When the $\omega C_P R_L$ value deviates from 0.1836 ($\varphi = -0.18\pi$ radian at the same time), there is a loss in class-E PA operation, degrading drain efficiency. We derived relationship between φ and $\omega C_P R_L$ as below,

$$\varphi = \frac{1}{2}\left[\sin^{-1}\left(\frac{\omega C_P R_L}{\sqrt{1/4 + 4/\pi^2}}\right) - \tan^{-1}\left(\frac{4}{\pi}\right)\right] \quad (2)$$

and there is an inverse proportion between φ and $\omega C_P R_L$. As $\omega C_P R_L$ increases, φ decreases, and transistor drain voltage is a positive value at $\omega t = 2\pi$. In contrast, as $\omega C_P R_L$ decreases, φ increases, resulting in negative transistor drain voltage at $\omega t = 2\pi$. A waveform of $v_C(\omega t)$ and $i(\omega t)$ in a single period is shown in Fig. 2 for different $\omega C_P R_L$ values. The transistor is on for $0 \le \omega t < \pi$ and off for $\pi \le \omega t < 2\pi$. When the ZVS is not satisfied ($\omega C_P R_L$ is not 0.1836), the voltage and current waveforms will overlap at the beginning of the next period, as shown in Fig. 2, because transient time is needed to have zero

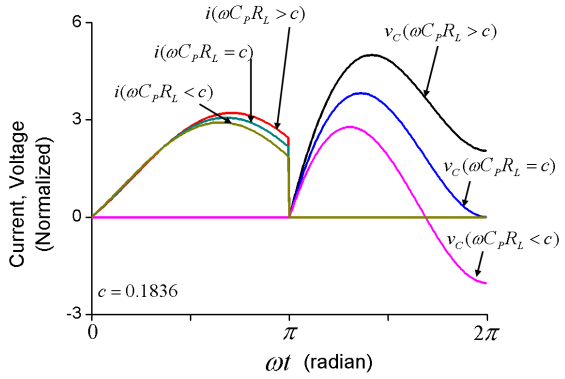

Fig. 2. Normalized voltage (on transistor drain) and current (flowing transistor) waveforms of class-E for different values of $\omega C_P R_L$.

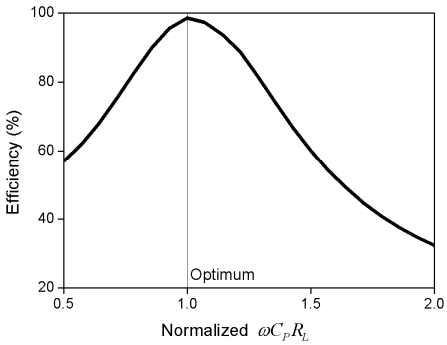

Fig. 3. Efficiency degradation according to normalized C_P deviation from optimum value (Q_{OUT}=20, R_L=5 Ω at 1.8 GHz).

voltage across the drain and source of the transistor. As a result, loss occurs during the transition. In Fig. 3, drain efficiency versus normalized $\omega C_P R_L$ is plotted, showing that efficiency degradation as $\omega C_P R_L$ deviates from the optimum value (normalized $\omega C_P R_L$=1.0). Therefore, to achieve high efficiency in class-E PA, C_P should be maintained with optimum value with a fixed R_L at a given frequency.

III. Negative Capacitance

As we have considered above, there is efficiency degradation as C_P deviates. However, in the field of CMOS PA, a large gate width is inevitable for delivering high output power. The gate widths are some millimeters wide and these wide transistors add pico farads capacitance on its drain node. We have shown efficiency degradation as C_P increases for a given output load and operation frequency in Fig. 3. C_P derivation from the optimum value prohibits lossless class-E PA operation and overlapping happens between the voltage on the transistor drain node and the current flowing transistor.

Because of the high peak voltage characteristic of a class-E PA, cascode topology is preferred for reliability. By stacking two transistors in series, voltage swings are divided into two transistors. However, additional common-gate (CG) transistors usually have large gate width to reduce on-resistance and this

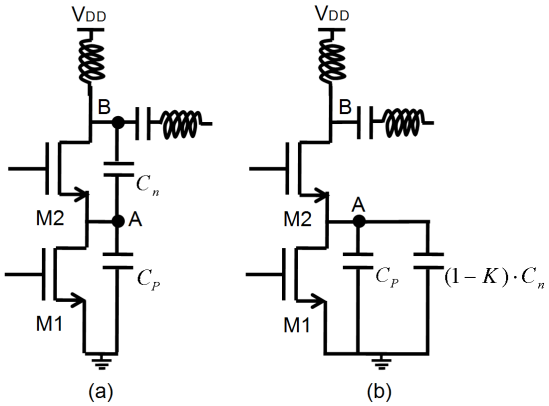

Fig.4. Schematic of (a) negative capacitance implementation, and (b) its equivalent circuit.

affects C_P increasing. Thus, as C_P increases over the optimum capacitance, more significant compensating for surplus capacitance is needed for efficiency enhancement.

To eliminate the surplus capacitance over the optimum C_P value, surplus capacitance tuning out is necessary. One of the techniques to tune out capacitance is to place an inductor on the same node with the DC block. However, this method contains several disadvantages. First, the inductor requires a large area to integrate on a single chip. In addition, as required inductance grows, the required area and inherent parasitic capacitances on the inductor are also increasing. Second, inductors are rarely tunable on a chip for mismatches and have a low quality factor (Q-factor) on an integrated circuit. If bonding wires are used for inductors with a higher Q-factor, it should be treated very delicately to control exactly.

Therefore, in this paper, we present a negative capacitance implemented by a capacitor using CG amplifier on cascode topology. Basically, negative capacitance works as polarity inversed Miller capacitance. Miller capacitance is stated as follows:

$$C_M = (1-K)\cdot C_n \qquad (3)$$

where K indicates voltage gain of the capacitor's nodes. Conventional C_M is applied with negative K, thus Miller capacitor increases capacitance ($1-K$) times more. On the contrary, the proposed negative capacitance is obtained using positive K. The implementation of negative capacitance is shown in Fig. 4 (a) noted as C_n. The nodes of capacitor (C_n) are connected to the source and drain of the CG transistor M2.

Since CG has a positive gain K, it generates negative capacitance C_M as described in (3). Its equivalent circuit is described in Fig. 4 (b). Using the Miller effect, C_n adds ($1-K$) times higher capacitance than C_n negatively on node A in Fig. 4. It decreases the surplus capacitance of node A adjusting C_P to optimum value, and restoring lossless class-E PA operation and efficiency. Also, C_n adjusts voltage stresses across the transistors. There is a large voltage stress on the CG transistor in a class-E power amplifier and its breakdown voltage limits the supply voltage V_{DD2}. Applying C_n alleviates large voltage

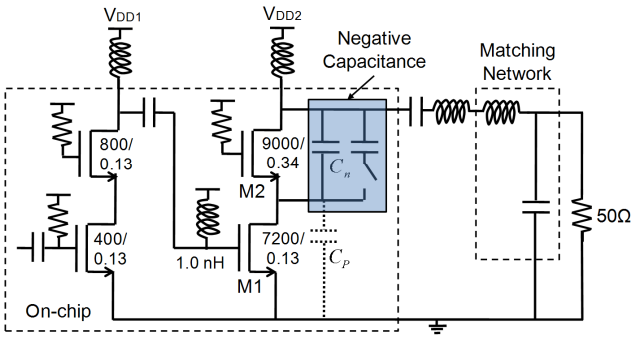

Fig. 5. Schematic of the proposed class-E PA including driver stage.

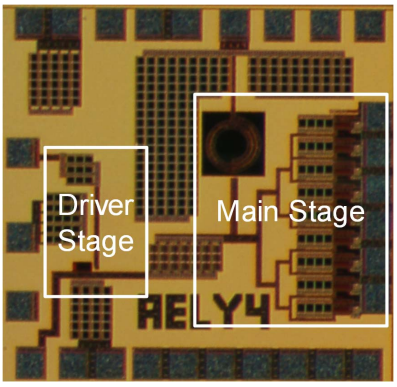

Fig. 6. Chip photograph of class-E PA including negative capacitance

stress on M2 balancing with M1. This increases voltage margin and improves transistor reliability from breakdowns.

Negative capacitance using a capacitor is profitable for integrated CMOS PA. A capacitor demands a much smaller space than an inductor and has a high Q-factor with less parasitic components. In addition, it is tunable arraying parallel capacitors with switches and requires a very small value thanks to CG gain K.

Parasitic capacitance on node B is not as much of a concern as that of node A because the value of parasitic capacitance on node B is smaller than that of node A. Furthermore, M2 is always turned on, so most of charging/discharging of capacitor occurs at node A according to the switching operation.

III. Circuit Design

A. Main Stage

A class-E amplifier has high peak voltage across the transistor and breakdown can occur on the CMOS transistor. In order to ensure reliability, we chose cascode topology, dividing voltage swing into two transistors [2].

For the standard 0.13-μm process, the foundry provided basically two different types of transistors: a thin gate-oxide transistor with a 0.13 μm gate-length for 1.2 V supply and a thick gate-oxide transistor with a 0.34 μm gate-length for 3.3 V supply. We stacked two different transistors for the best performance. The thin gate-oxide transistor is used for common-source (CS) transistor M1 and the thick gate-oxide transistor is used for CG transistor M2 (Fig. 5). This combination works better than two thick gate-oxide transistors in the aspects of RF performance and on-resistance.

The thin gate-oxide transistor shows better RF performance than the thick gate-oxide transistor and this alleviates driver stage design complexity. Additionally, it contains smaller parasitic capacitance that augments drain capacitance and has smaller on-resistance. The gate width is determined to drive sufficient current for output power. In this work, a 7200 μm gate-width was implemented. On the M1 gate bias circuit, we used an inductor as a gate bias circuit, resonating with input gate capacitance on M1 to drive the CS transistor efficiently.

The thick gate-oxide transistor for M2 is sustainable for high peak voltage. M2 should endure the voltage stress to prevent gate-drain (GD) breakdown. This CG transistor is biased to be in the on-state all times. This is intended to maintain low on-resistance, thus enabling the maintenance of high efficiency. For implementation, we used 9000 μm gate-width transistor.

C_n is connected to two nodes, across the drain and source of M2. There is trade-off between the value of C_n and stability because C_n can give a feedback loop on CG. However, thanks to CG amplifier gain K, negative capacitance works at $(1-K)$ times higher than actual capacitance C_n, thus a small value of C_n is needed and it does not hurt stability. In our design, we used a 900 fF capacitor to compensate for surplus C_P. On design simulation assisted by the Advanced Design System, we could not see any obvious stability degradation. Besides, this scheme does not need an external circuit to generate negative capacitance in single-ended schematic, so it is very simple to implement.

B. Driver Stage

In the driver stage, a class-E driver amplifier is implemented. Since a class-E amplifier has high peak voltage, we can drive the main amplifier sufficiently with low supply voltage V_{DD1}. This reduces PAE degradation caused by driver stage DC consumption. In this way, PAE is only about 3% to 4% lower than drain efficiency (DE). Here, we also adapted cascode topology to ensure reliability from breakdowns. Gate width of 400 μm and 800 μm with gate-length 0.13 μm transistors are used for CS and CG, respectively.

IV. Implementation and Measurement Results

The PA including the driver stage is fabricated using a 0.13-μm standard CMOS process. A die photograph is shown in Fig. 6. The die area is 0.97 mm^2 including bonding pads. DE and PAE measured versus main supply voltage V_{DD2} are plotted in Fig. 7, along with output power at 1.8 GHz. V_{DD2} varies from 0.3 V to 3.3 V. On measurement, 29 dBm output power was measured at a supply voltage of V_{DD2}=3.3 V, with 66% DE and 63% PAE. The driver stage consumes about 50 mW with V_{DD1}=1.2 V. During the test, the input signal was set to 2.5 dBm, so 26.5 dB power gain is achieved.

We placed multiple bonding pads to minimize bonding inductance variation. Six pads were implemented for the

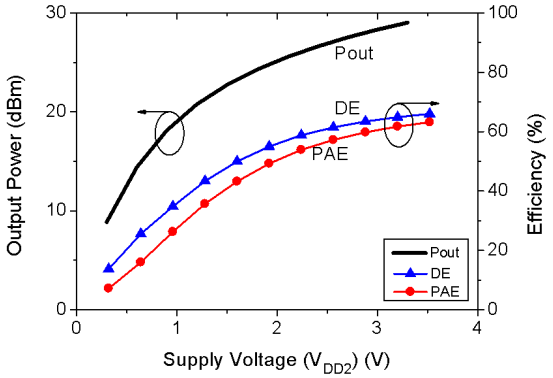

Fig. 7. Output power, DE and PAE versus supply voltage V_{DD2}.

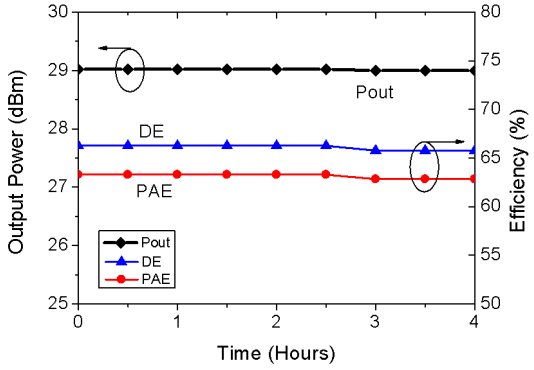

Fig. 8. Output power, DE and PAE versus time.

output node and 14 pads for the ground. Parasitic capacitance from multiple pads is compensated by considering capacitance values.

To demonstrate the reliability of our cascode class-E PA, we operated the PA at maximum output power for a long time. For four hours, we checked output power, DE and PAE, maintaining V_{DD2}=3.3 V. As shown in Fig. 8, we cannot see output power and efficiency degradation. Output power dropped only 0.02 dB and DE and PAE dropped just 0.5% after four hours of operation.

Finally, the performance of the presented class-E PA in this work is compared to published single-ended switching CMOS power amplifiers (see Table I). Output power of Ref. [5] is higher but it uses an extended-drain NMOS device whose breakdown voltage is 15 V and 4.8 V was applied as V_{DD}. PAE of Ref. [3] is higher than in this work, but this work shows much higher output power (resulting from efficiency-output power tradeoff). Class-E PA is switching amplifier, so constant envelope modulation signals are suitable. To test this PA, we applied GMSK modulated signal with BT=0.3 and measured error vector magnitude (EVM) 0.6% with 29 dBm output power.

V. Conclusion

In this paper, a novel scheme compensating for surplus parasitic drain capacitance on a class-E is proposed. The proposed power amplifier including negative capacitance is implemented with simplicity by using a capacitor with CG amplifier on cascode topology. This amplifier delivers 29 dBm with 66% DE and 63% PAE at 1.8GHz without harming stability, using a 0.13-µm standard CMOS process. There is almost no performance deterioration for four hours of maximum power operation.

TABLE I
Comparison of CMOS PAs.

Reference	Process (nm)	Freq. (MHz)	P_{OUT} (dBm)	PAE (%)
[2]	250	900	29.5	41
[3]	130	1700	23	67
[5]	65	2000	30	60
This work	130	1800	29	63

Acknowledgments

This work was supported by the Korea Science and Engineering Foundation (KOSEF) through the National Research Lab. Program funded by the Ministry of Education, Science and Technology (No. ROA-2007-000-20118-0(2007)).

References

[1] K.-C. Tsai and P. R. Gray, "A 1.9-GHz, 1-W CMOS Class-E Power Amplifier for Wireless Communications," *IEEE Journal of Solid-State Circuit,* vol. 34, pp. 962-970, Jul. 1999.

[2] C. Yoo and Q. Huang, "A Common-Gate Switched 0.9-W Class-E Power Amplifier with 41% PAE in 0.25-µm CMOS," *IEEE Journal of Solid-State Circuits.* vol. 36, no. 5, pp. 823-830, May 2001.

[3] A. Mazzanti, L. Larcher, R. Brama, and F. Svelto, "Analysis of Reliability and Power Efficiency in Cascode Class-E PAs," *IEEE Journal of Solid-State Circuits.* vol. 41, pp. 1222-1229, May 2006.

[4] R. Brama, L. Larcher, A. Mazzanti, and F. Svelto, "A 30.5 dBm 48% PAE CMOS Class-E PA with Integrated Balun for RF Applications," *IEEE Journal of Solid-State Circuits.* vol. 43, pp. 1755-1762, Aug. 2008.

[5] M. Apostolidou *et al*, "A 65nm CMOS 30dBm Class-E RF Power Amplifier with 60% Power Added Efficiency," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 141-144, Jun. 2008.

[6] F. H. Raab, "Idealized Operation of the Class E Tuned Power Amplifier," *IEEE Trans. Circuits Syst.,* vol. 24, pp. 725-735, Dec. 1977.

[7] A. Grebennikov, and N. O. Sokal, *Switchmode RF Power Amplifiers.* Burlington, MA: Newnes, 2007.

[8] N. O. Sokal, "Class-E Power Amplifiers" *QEX/Communications Quarterly*, pp. 9-20, Jan./Feb. 2001.